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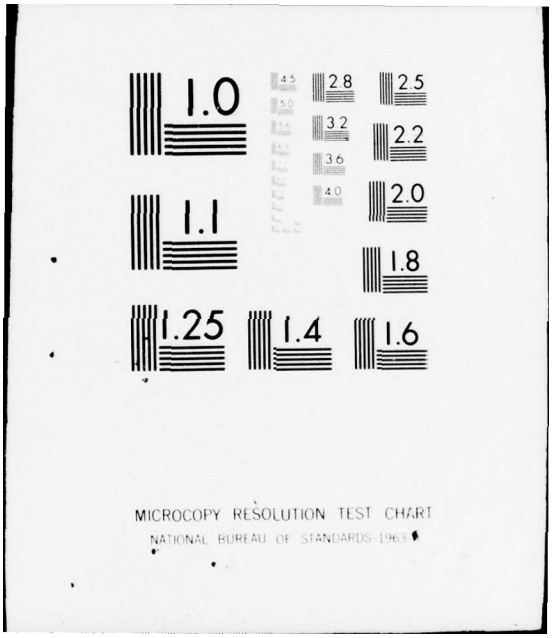
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GALLIUM ARSENIDE VERTICAL CHANNEL INSULATED GATE FIELD-EFFECT TRANSISTOR

M. C. Driver, D. A. Tremere and D. L. Barrett

Annual Report
1 February 1977

Contract N00014-75-C-0418
Contract Authority No. NR 251-019

Office of Naval Research
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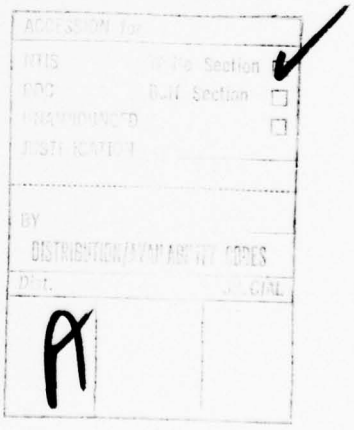
ABSTRACT

The technologies necessary to fabricate a power microwave frequency, vertical channel, gallium arsenide insulated gate field-effect transistor have been further developed. Planar devices that show FET action have been fabricated. The etching technology for a V-groove version of the vertical channel device has been explored.



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1. INTRODUCTION

The overall objective of the program is to investigate the feasibility of developing a vertical n-channel enhancement mode insulated gate field-effect transistor device in gallium arsenide which is ultimately capable of delivering up to 5W of power (Class A) and which has a minimum power gain of 6 dB over the frequency range from 4 to 8 GHz. Additional design goals for these devices are that they should be linear in phase ($\pm 5°$ deviation) and gain (third order IMD < -20 dB) at these frequencies and over the whole dynamic range of operation.

Work during this period has been concentrated on the technologies necessary to fabricate a planar MISFET as a first step towards a vertical channel device. The report is divided up into two broad areas:

(1) MIS Technologies:

(a) The necessary doping profiles for the planar device have been produced by ion implantation (sulfur) and vapor phase epitaxy. The devices fabricated from this latter method have shown more promise. The epitaxial development has continued to the point where p-type layers can be grown by the addition of diethyl zinc to the hydrogen carrier gas. Heavily doped n-type layers are grown by the addition of sulfur or tin chloride to the hydrogen carrier gas stream.

(b) An empirical mathematical model for the anodization process has been developed. In addition to its application for producing the gate oxide, anodization has been used as a very effective means of thinning epitaxial layers and at the same time "staining" them.

(2) Device Fabrication:

(a) Etches suitable for the fabrication of mesas on the epitaxial material have been developed. Five wafers of gallium arsenide have been processed, giving much needed experience. Working devices were fabricated which showed FET action even before the anodic oxide annealing process. These devices remain to be further optimized.

(b) A V-groove device is planned as the next step and the etching technology has been investigated and mask design completed.

2. PROCESS TECHNOLOGIES

2.1 Ion Implantation

P^+-type implants are required in the fabrication of the vertical channel device as a means of grounding the p-channel substrate of the device to the source contact. This can readily be seen by reference to Fig. 1 which shows the fabrication sequence of the VMIST device on an epitaxial structure.

Zinc implants were reported in last year's annual report when it was shown that implantation into chromium doped gallium arsenide substrates apparently yielded activation efficiencies of 400%. To resolve this problem, Zn^{++} implants were made into lightly doped n-type epitaxial layers on semi-insulating substrates at an effective energy of 300 KeV, and at dose levels of $5 \times 10^{14}/cm^2$ and $5 \times 10^{13}/cm^2$. The samples were encapsulated with sputtered SiO_2 and annealed in a nitrogen ambient at 725°C. The results are summarized in Table I.

TABLE I

Dose Level	Anneal Time	Activated Q	Mobility	Activation Efficiency
5×10^{14}	60 min	2.9×10^{14}	79.4	60%
5×10^{13}	60 min	1.1×10^{13}	140.5	23%
5×10^{13}	240 min	3.4×10^{13}	130.0	69%

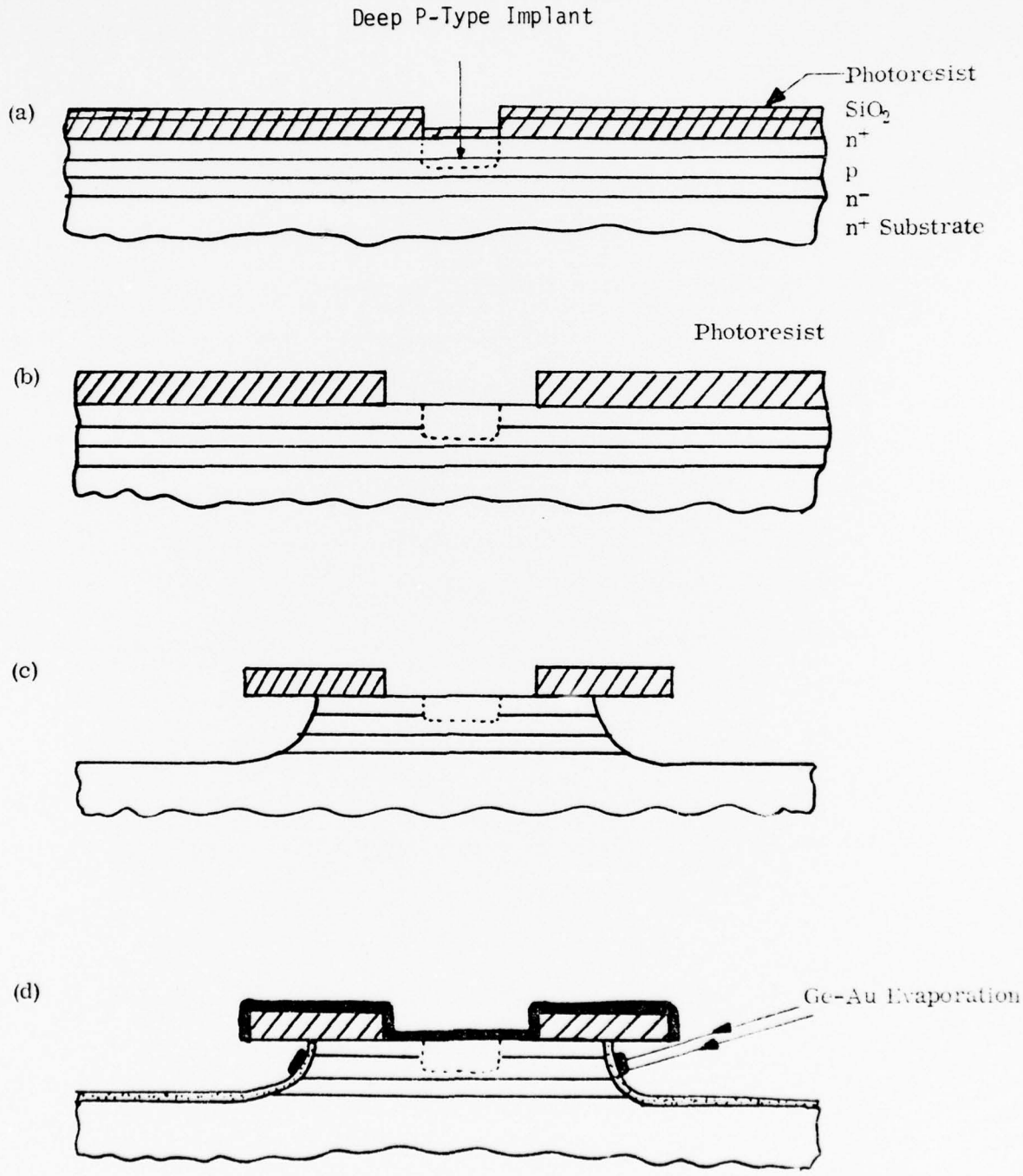


Figure 1 — VMIST fabrication steps.

2.2 Wafer Profiling

A technique to measure the profile of the implanted zinc concentration with depth into the sample using the Differential Hall Effect has been developed. This involves removing the surface of the semiconductor a little at a time and measuring the Hall mobile charge and mobility after each removal to obtain the carrier profile. All of the implants to date have been shallow ($\sim$1000Å), and in order to obtain a sufficient amount of data to measure the profile accurately, the surface must be removed in 100Å steps. To do this, the area between the contacts of the Hall sample is anodized and subsequently etched away to remove the gallium arsenide in small steps.

The anodizing solution is the standard composition of 3 gms of sodium citrate in 100 cc of water mixed with 100 cc of ethylene glycol and buffered with citric acid to a pH of 5.5. The oxide film is not removed between measurements but is allowed to accumulate in thickness as the anodizing voltage is raised for each step between Hall measurements. The advantage of this is that the color of the film enables its thickness to be estimated by comparison with separate "standard" samples to an accuracy of better than 20Å. The presence of the oxide has been shown to have no effect on the Hall measurements. The zinc implanted samples have been evaluated very successfully in this manner and one of the results is shown in Fig. 2.

(The apparent increase in carrier density at the surface of the sample is interesting and unexpected, but time has not allowed further studies.)

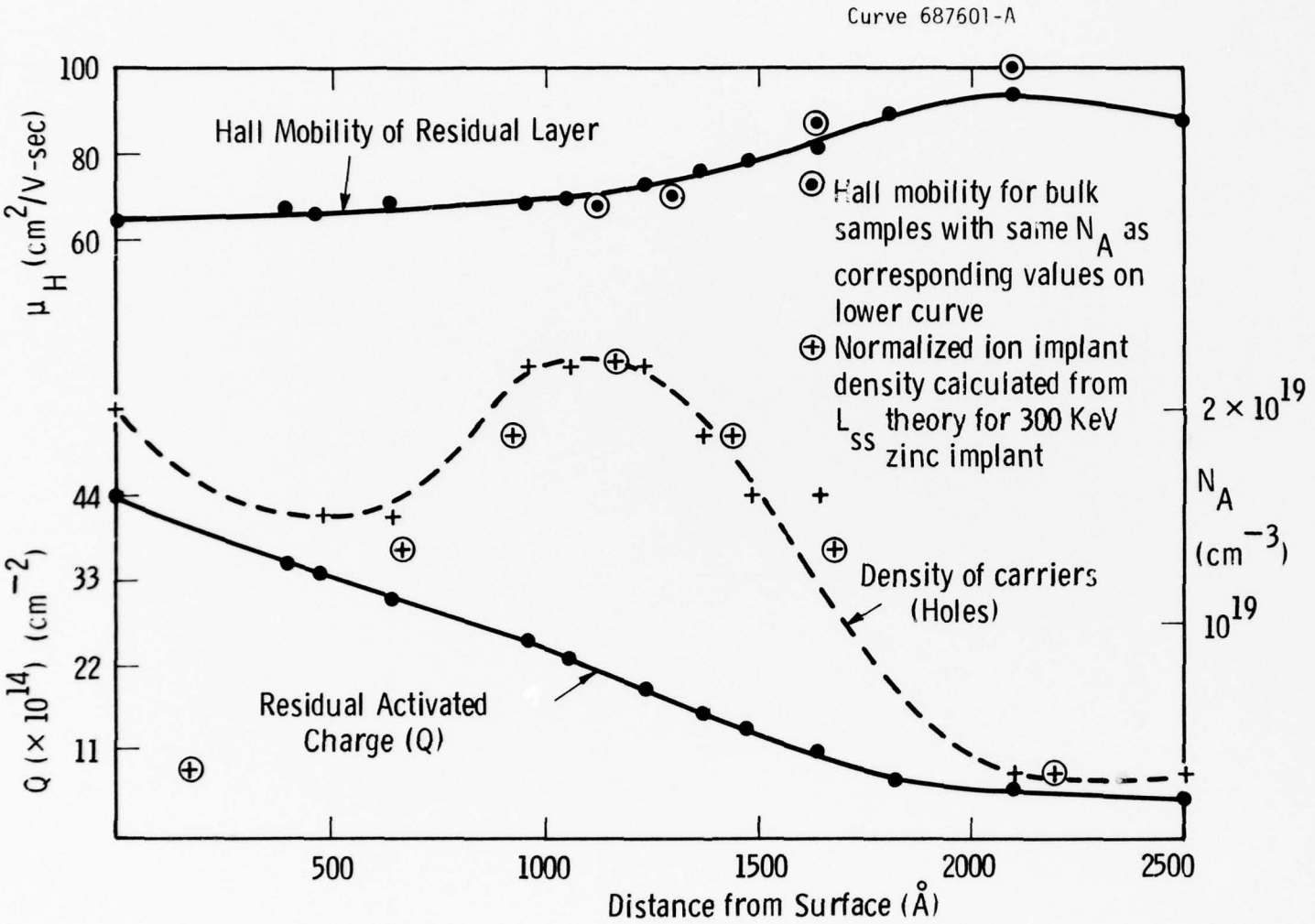


Fig. 2 – Impurity distribution of Zn^{++} implantation

The residual activated charge was calculated from the Hall measurements after each anodization step and is plotted as a function of distance from the surface.

Since the implanted charge Q(x) is given by

$$Q(x) = \int_{\infty}^{x} N_A(y)dy$$

and

$$\frac{dQ(x)}{dx} = N_A(x),$$

the slope of the residual activated charge, therefore, gives the density of activated charge centers. This is also shown plotted in Fig. 2. The circled points are obtained from the LSS theory for 300 KeV zinc ions implanted into gallium arsenide. The curve for these theoretical points has been normalized to the maximum of the measured distribution and shows a reasonably good fit to the experimental points. Also in Fig. 2 is plotted the Hall mobility of the residual (implanted) layer, and included for comparison are bulk Hall mobilities for the measured carrier concentration profile. The implanted Hall mobility values appear to be very reasonable. The comparison has not been extended to the surface of the sample until the surface concentration 'pile-up' effect has been established by further studies.

The result of the studies made so far on zinc implantation indicate that, unless the energy of the implanted species can be increased above the 300 KeV limit set by the apparatus at the present time, it may not be possible for the zinc doping to extend the necessary

1 μm into the p-type substrate even with a prolonged diffusion. Experiments are underway to investigate this and to study the penetration and suitability of the lighter beryllium atom.

2.3 Anodization Studies

2.3.1 Anodization Model

A mathematical model for the formation of the anodic oxide on gallium arsenide has been constructed which enables us to predict the thickness of the oxide under both constant current and constant voltage bias conditions. The analysis also enables us to calculate the rate at which the anodization solution etches the oxide (and hence the gallium arsenide).

The equations governing the oxide behavior are:

Rate of Oxide Growth

$$\frac{dW}{dt} = \frac{J}{\beta} - \varepsilon \qquad (1)$$

where $\beta = 1.8 \times 10^4$ coulombs per cm^2 is the growth constant and ε is typically 1.4×10^{-2} Å per second.

Current-Voltage Characteristic

Initial calculations were made with the relationship

$$J = (E_c/\rho)\cdot(V/(E_cW - V)) \qquad (2)$$

where E_c is the critical field in the oxide, equal to 5.03×10^6 V/cm, and ρ is the low field resistivity, equal to 1.3×10^{13} ohm-cm.

The two equations combined to give quite a good fit to the experimental curves governing the rate of anodic current decay at constant voltage.

A much better fit was obtained using the relationship

$$J = J_c \exp \frac{\gamma}{W} (V - E_c W) \qquad (3)$$

which is similar to the form $J = 2K_1 \text{ sink } (K_2 V)$ given by Young.[2]

The constants have the following empirically determined values:

$$\gamma = 3.39 \times 10^{-6} \text{ cm/V}$$

$$J_c = 10^{-4} \text{ amps.}$$

A comparison of the fit to the experimental points of the calculated curves for the two J-V characteristics is shown in Fig. 3.

2.3.2 Anodization Procedures

The sequence of operations for anodizing a wafer is as follows: A constant current is applied to the sample and as the oxide grows on the surface, the voltage developed across the sample increases until it reaches the required value whereupon it is held constant and the current allowed to decay. The growth of the oxide during this initial period at constant current (J_A) is governed simply by equation (1)

$$W = (J_A/\beta - \varepsilon)t$$

or when the required voltage V_A is reached

$$W_A = V_A/(E_c + \frac{1}{\gamma} \log_e (J_A/J_c))$$

This is the initial thickness of the film when the current starts to decay and in Fig. 3 is put equal to 10^{-3} amps/cm^2. The series resistance

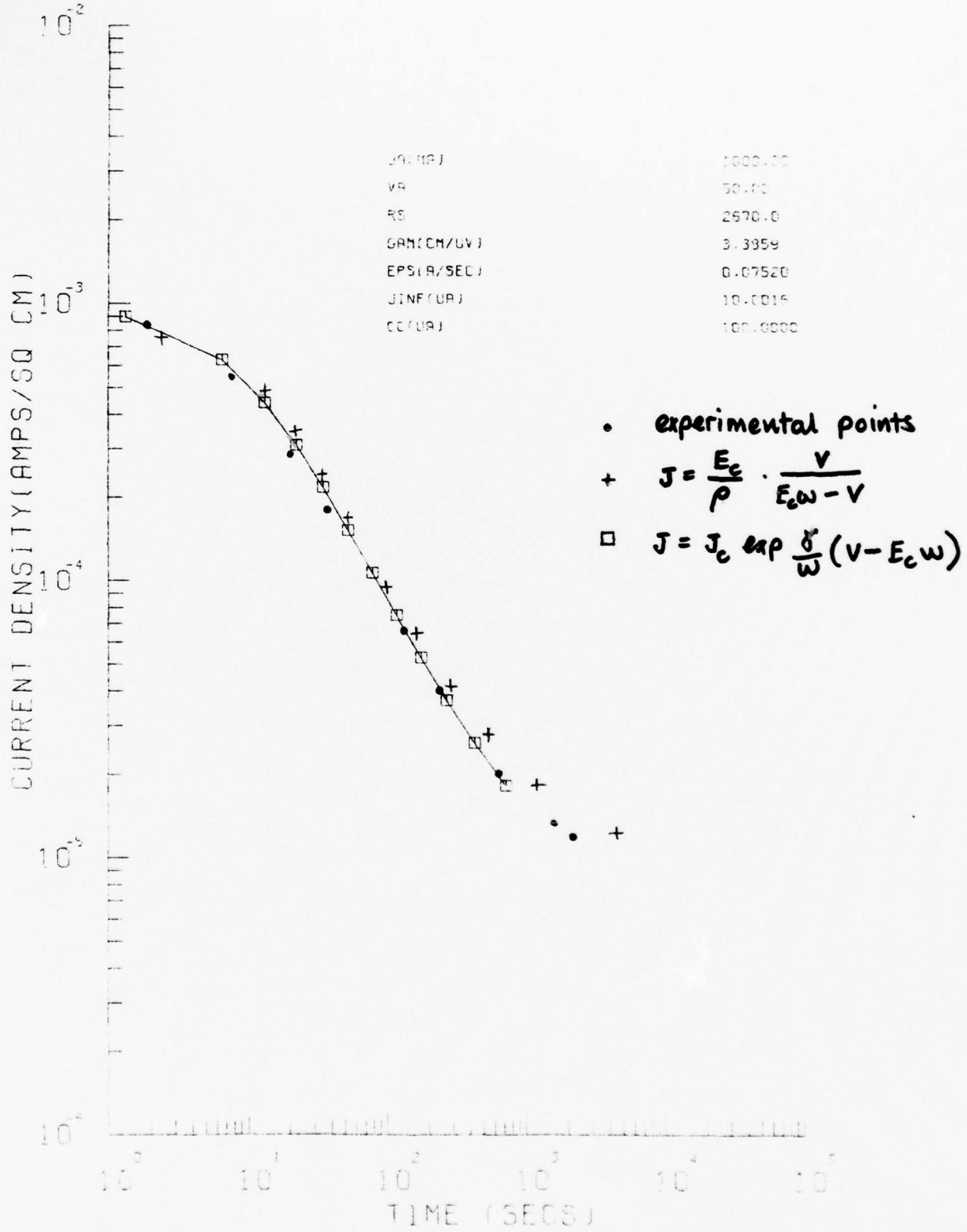


Figure 3 - Anodic Current Density Decay with Time at Constant Voltage.

in the circuit (sheet resistance of the sample plus solution resistance) is 2.67 KΩ, the etching rate for the self-etching of the anodic oxide in the solution is .0752Å/sec, leading to a saturation anodization current at infinite time of 10 mA/cm^2.

The calculation enables us to determine the oxide thickness accurately. In Fig. 4, it can be seen that the growth of the oxide under constant applied voltage is nonlinear and is far from its final thickness value when the current first starts to decay. This information about the time dependence of oxide thickness is very valuable when accurate removal of gallium arsenide material by anodization is required.

2.4 Vapor Phase Epitaxy

Vapor epitaxial growth techniques have been developed to prepare the epitaxial GaAs VMIST structures according to the following scheme.

n^+	1 μm	10^{18} cm^{-3}
p	1 μm	mid 10^{16} cm^{-3}
n^-	3-4 μm	$<10^{15}$ cm^{-3}
	Drift Region	
n^+	substrate	

Starting with <100> oriented substrates which are silicon doped with net carrier concentration near 10^{18} cm^{-3}, the wafers are lapped with alumina and chem-mechanically polished in an acid-peroxide solution to obtain specular, damage-free surfaces. A cleaning etch is

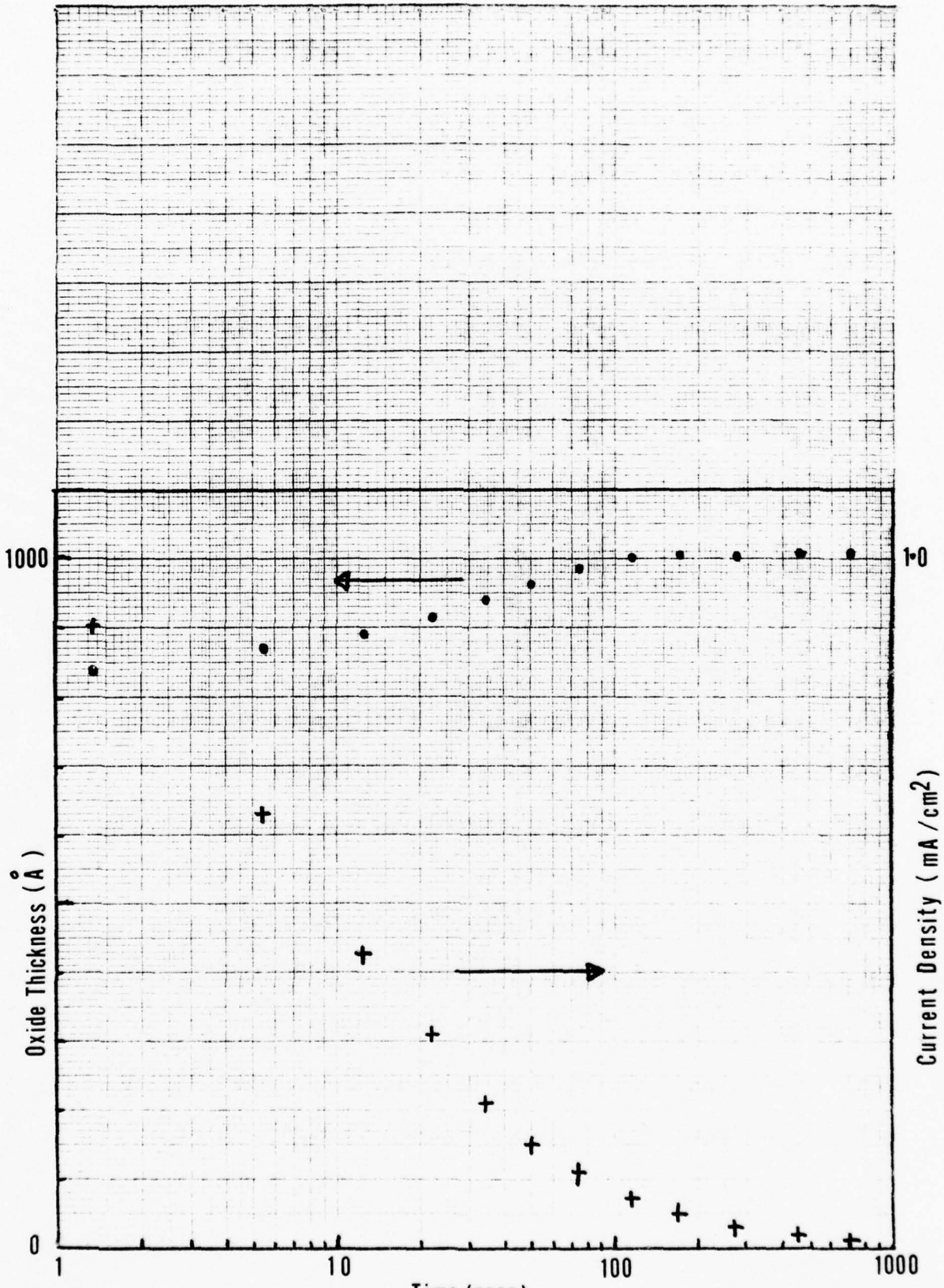


Figure 4 - Oxide Thickness Vs. Time.

used immediately before loading in the epitaxial reactor, and an in-situ etch is used immediately prior to epitaxial deposition to yield good epitaxy and a low defect interface region.

Epitaxial layers are grown using the $AsCl_3/Ga/H_2$ technique in the substrate holder shown in Fig. 5a and in the epitaxial reactor system shown in Fig. 5b. The system is schematically shown in Fig. 5c. Using a combination of clean techniques and pure source materials with a high mole fraction of $AsCl_3$ (mole fraction control) undoped epitaxial layers on n^+ substrates have been grown with carrier concentrations less than 10^{13} cm^{-3}. An example is shown in the concentration profile of Fig. 6 obtained by the CV profiling technique. The zinc doped p-layer was grown on this profile by the addition of a dilute vapor of diethyl zinc to the hydrogen gas stream through the epitaxial reactor. The diethyl zinc is a pyrophoric organometallic compound which was obtained in 5 nines purity from Alfa Products (Danvers, MA). Since this compound is a liquid with a significant vapor pressure at room temperature ($\sim$15 mm), it was cooled down to about -20°C to give vapor pressures suitable for doping. Figure 7 shows the vapor pressure of $(\varepsilon\tau)_2$ Zn as a function of temperature in the range of interest. Hydrogen gas is metered and bubbled through the diethyl zinc liquid to become saturated with the vapor at the thermostated temperature. This gas mixture enters the hot reactor where the diethyl zinc decomposes at higher temperature. Doping occurs by incorporation of zinc into the GaAs epitaxial layer at an acceptor level of 0.024 eV.

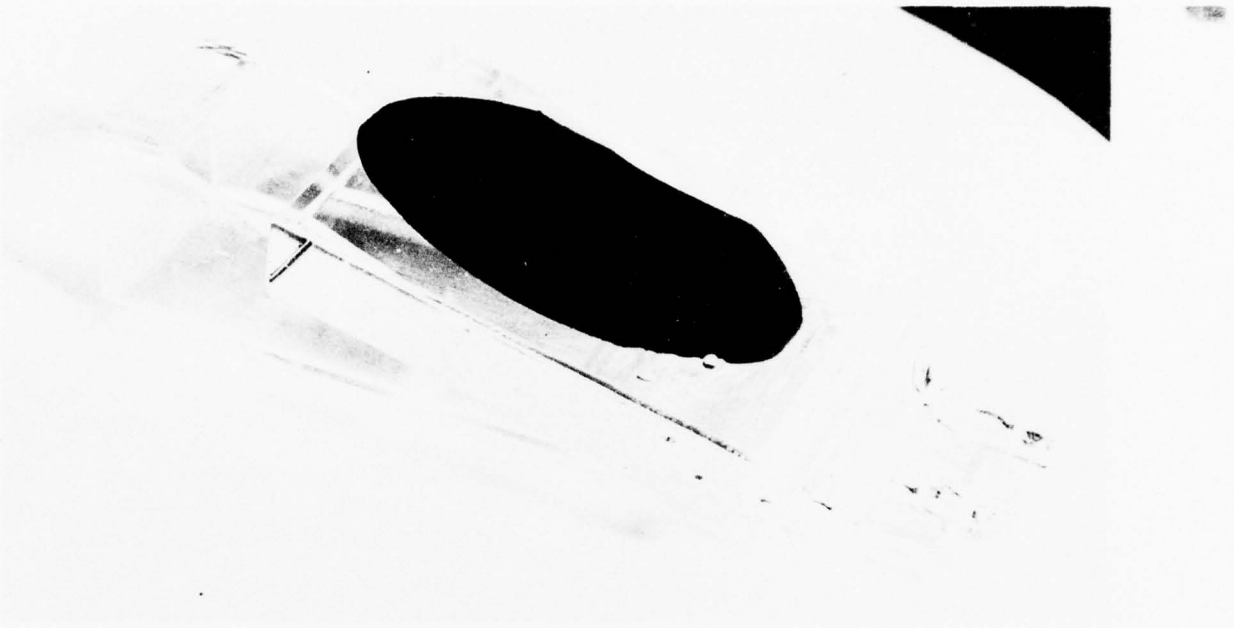


Figure 5a - Substrate holder.

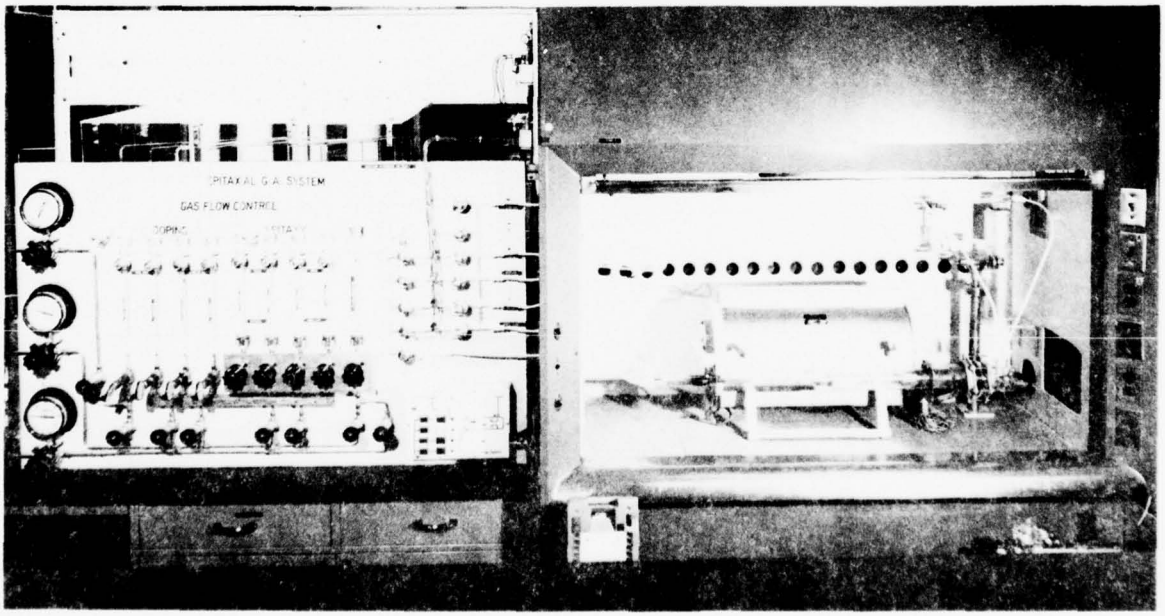


Figure 5b - VPE reactor.

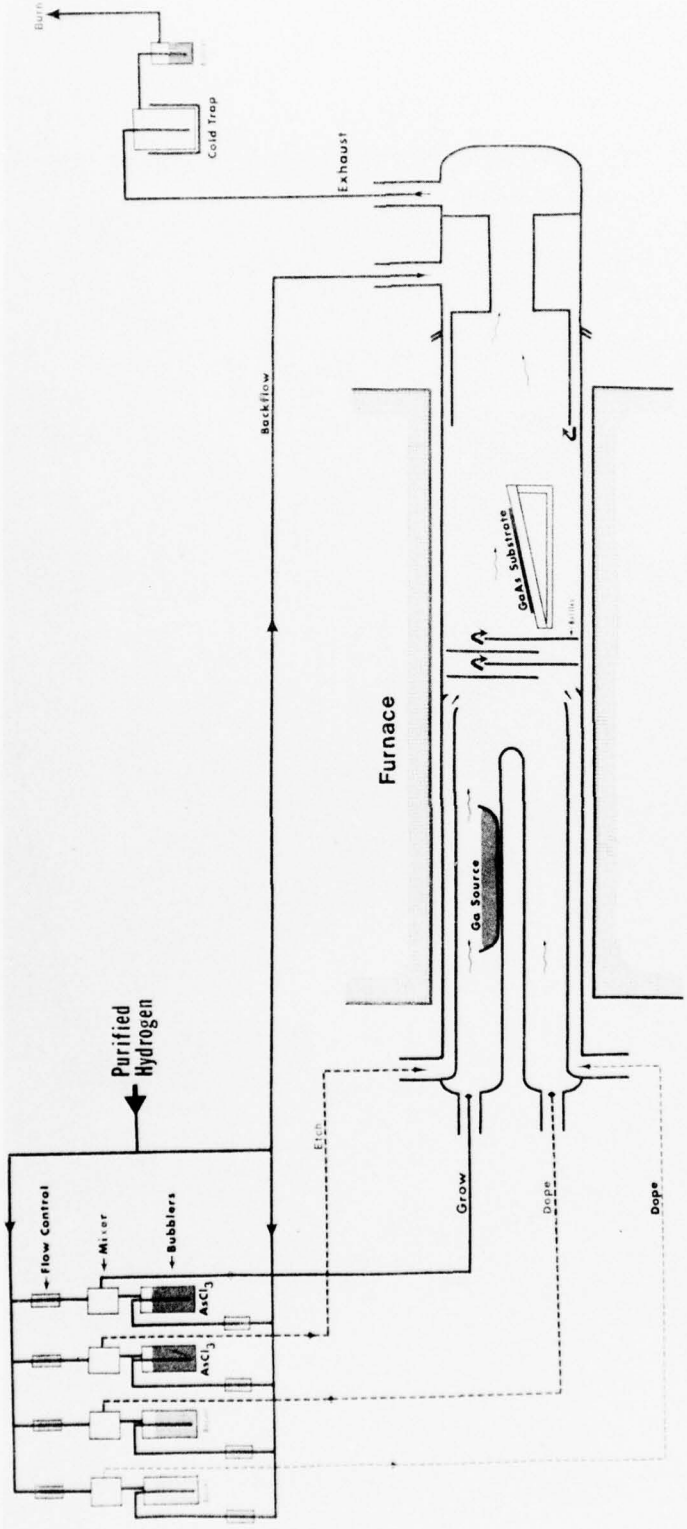


Figure 5c - VPE reactor system.

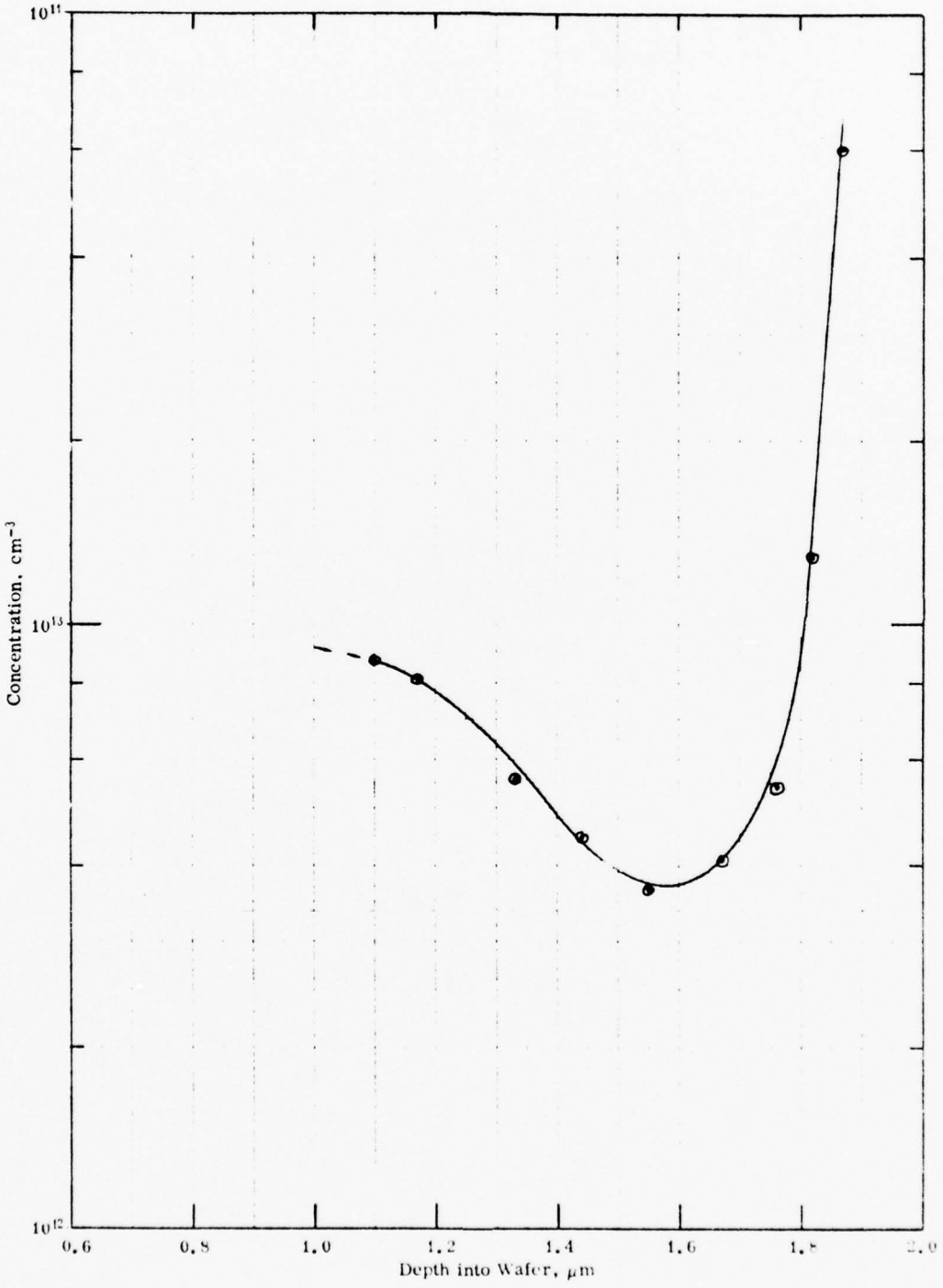


Figure 6 — N^- epitaxial profile in GaAs.

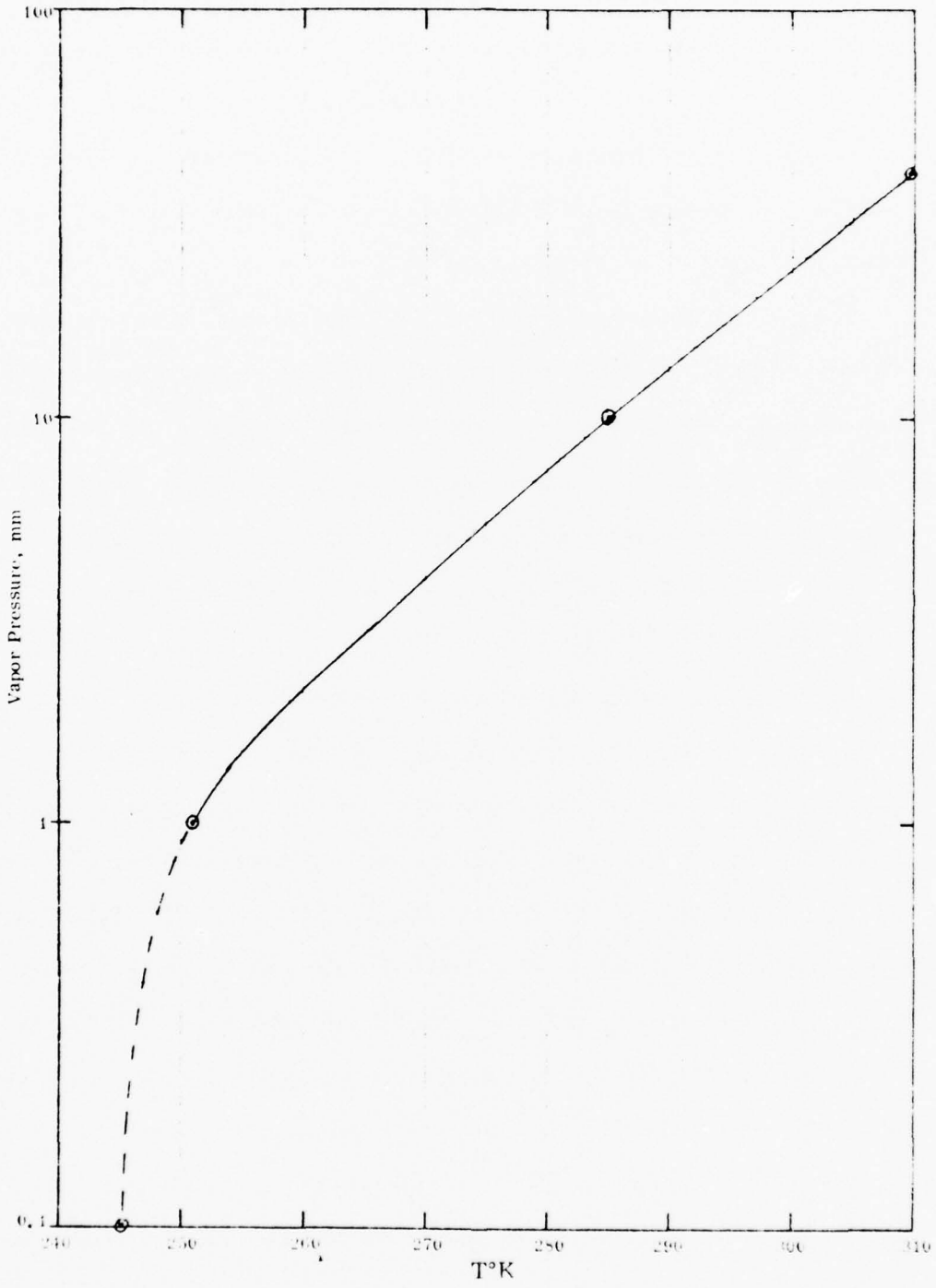


Figure 7 – Vapor pressure of diethyl zinc.

Zinc doped p-type layers have been grown on n^+ substrate and on n^- on n^+ substrates in thicknesses of 0.5 to 6 μm, and concentrations from 6×10^{15} to 8.5×10^{17} cm^{-3}. The optical micrograph of Fig. 8 shows the stained cross section of a $p\text{-}n^-\text{-}n^+$ structure. The top layer is a 1.7 μm thick p-layer which is followed by an n^- layer of 5 μm thickness grown on an n^+ substrate.

From these preliminary doping experiments, mole concentration of Zn deposit flows and experimentally measured (capacitance-voltage) carrier concentrations have been determined. These values are plotted in Fig. 9. A fairly good correlation between these two parameters has been obtained by keeping all other growth parameters constant.

Sulfur doped n^{++} layers were grown by incorporating sulfur vapor from a heated sulfur source. For n^{++} doped layers ($\sim 10^{18}$ cm^{-3}) elemental sulfur having a low vapor pressure was heated to near 110 to 112°C in a thermostated vessel in close proximity to the reactor, and hydrogen was passed through the vessel to transport the sulfur vapor to the deposition zone. At present, the calibration of the n^{++} concentration with solid sulfur temperature are incomplete. Experiments were also made to prepare tin doped n^{++} layers by bubbling hydrogen carrier gas through tin chloride liquid thermostated at -20°C. The high vapor pressure over tin chloride produced n^{++} layers with concentrations in excess of 10^{18} cm^{-3}. A preliminary attempt was made to grow an (n^+) - (p) - (n^-) - (n^+ substrate) device structure combining the epitaxial growth and doping techniques using diethyl zinc and solid sulfur. This structure is shown in the micrograph of Fig. 10. In this cross section, the n^+ layer is 2.8 μm, the p layer 3.5 μm, and the n^- drift region 2.8 μm.

Figure 8 — Optical micrograph of $p\text{-}n^{-}\text{-}n^{+}$ epitaxial wafer CD3-R43-2 cross section (1700 X).

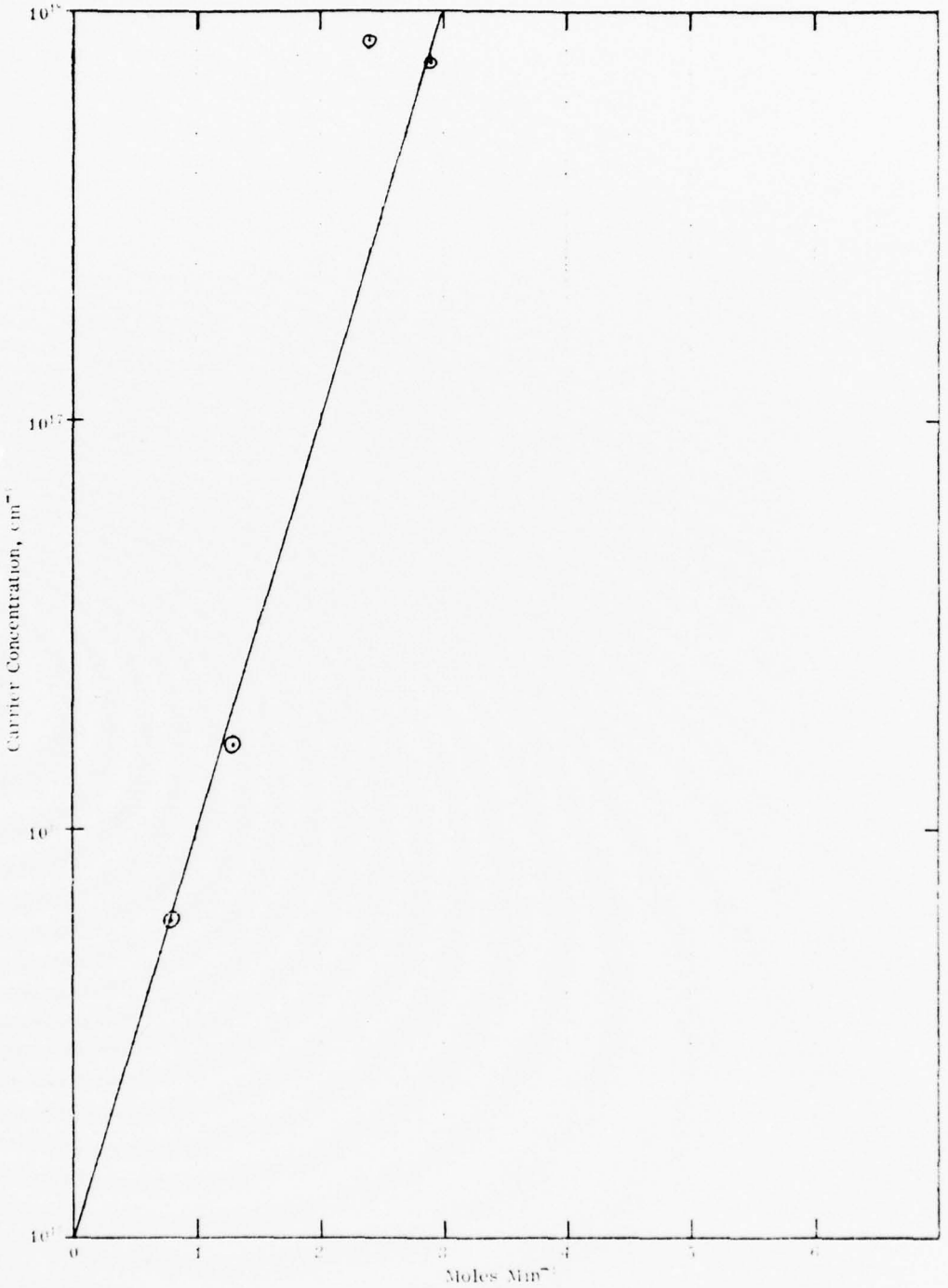


Figure 9 — Carrier concentration with flow of diethyl zinc dopant.

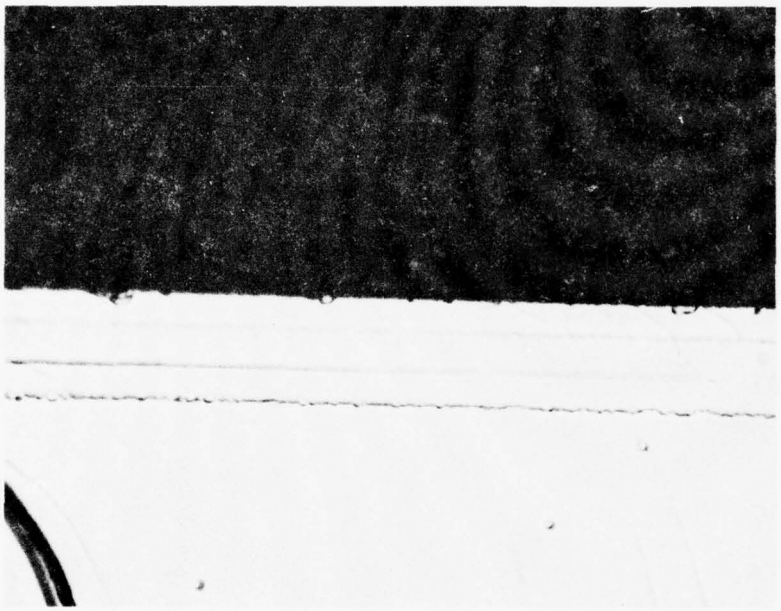


Figure 10 - Photomicrograph of n^+-p-n^--n^+ epitaxial wafer CD3-R38-1 (1700 X).

3. DEVICE FABRICATION

3.1 Introduction

A cross section of a planar (MISFET) device is shown in Fig. 11. Here the heavily doped n-type ($N_d \sim 10^{19}/cm^3$) contacts for the source and drain of the device have been formed by ion implantation of S or Si. In Fig. 12 is shown the same device with source and drain mesa contacts formed from etching back an n-type epitaxial layer on top of the p-type substrate. Both of these approaches have been used but the success and availability of good n-type layers have led us to favor the mesa approach.

3.2 Mesa Etching

The height of the mesas was chosen to be 1 micron. This is a compromise between the sheet resistance of this contact (from contact metal to channel) and the step over which the gate, source and drain metallizations must be continuous.

The etching mask used for the mesa definition is Waycoat IC resist[3] but it was found necessary to treat the gallium arsenide surface to a pretreatment (AP100)[4] in order to improve the adhesion of the resist during the etching step.

The requirement on the etch is that the surface of the etched region should be at least as good as the original surface (polishing etch). In addition, the etch rate should not be too fast so that control

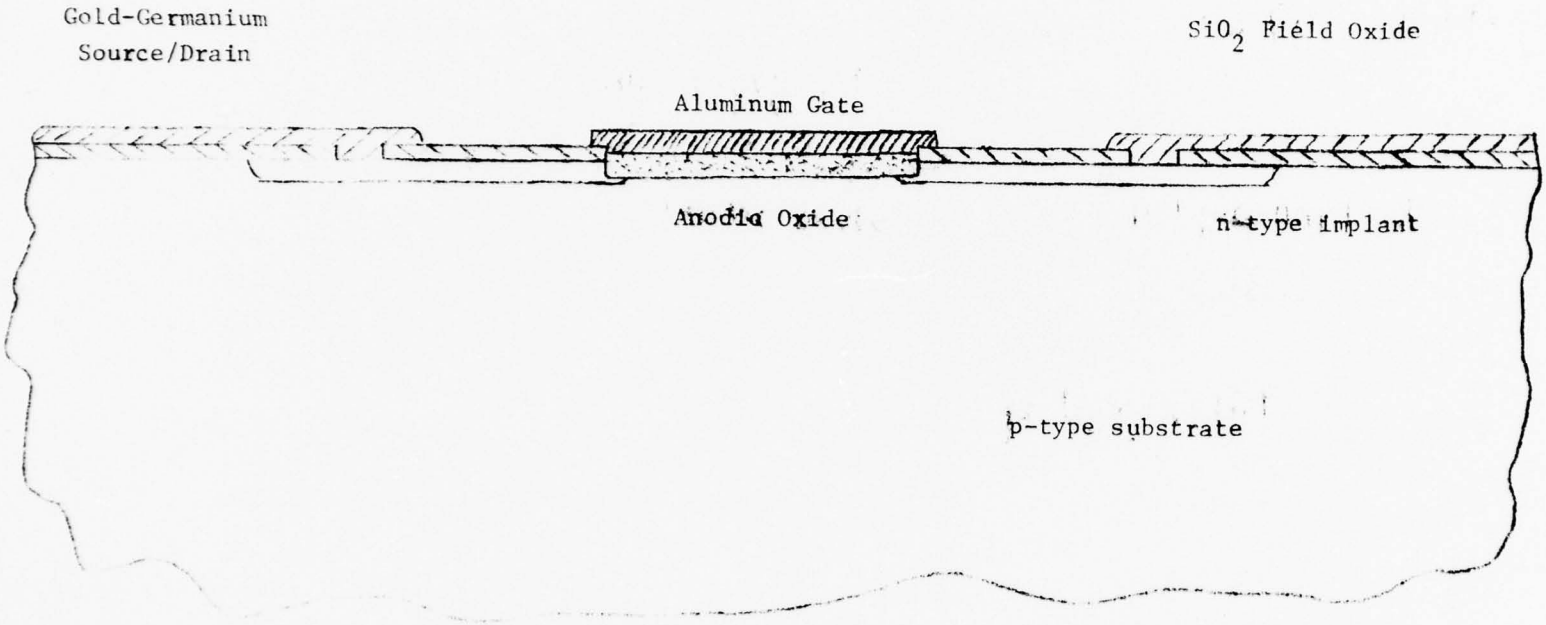


Figure 11 - Planar MISFET formed by ion implantation of source and drain contacts.

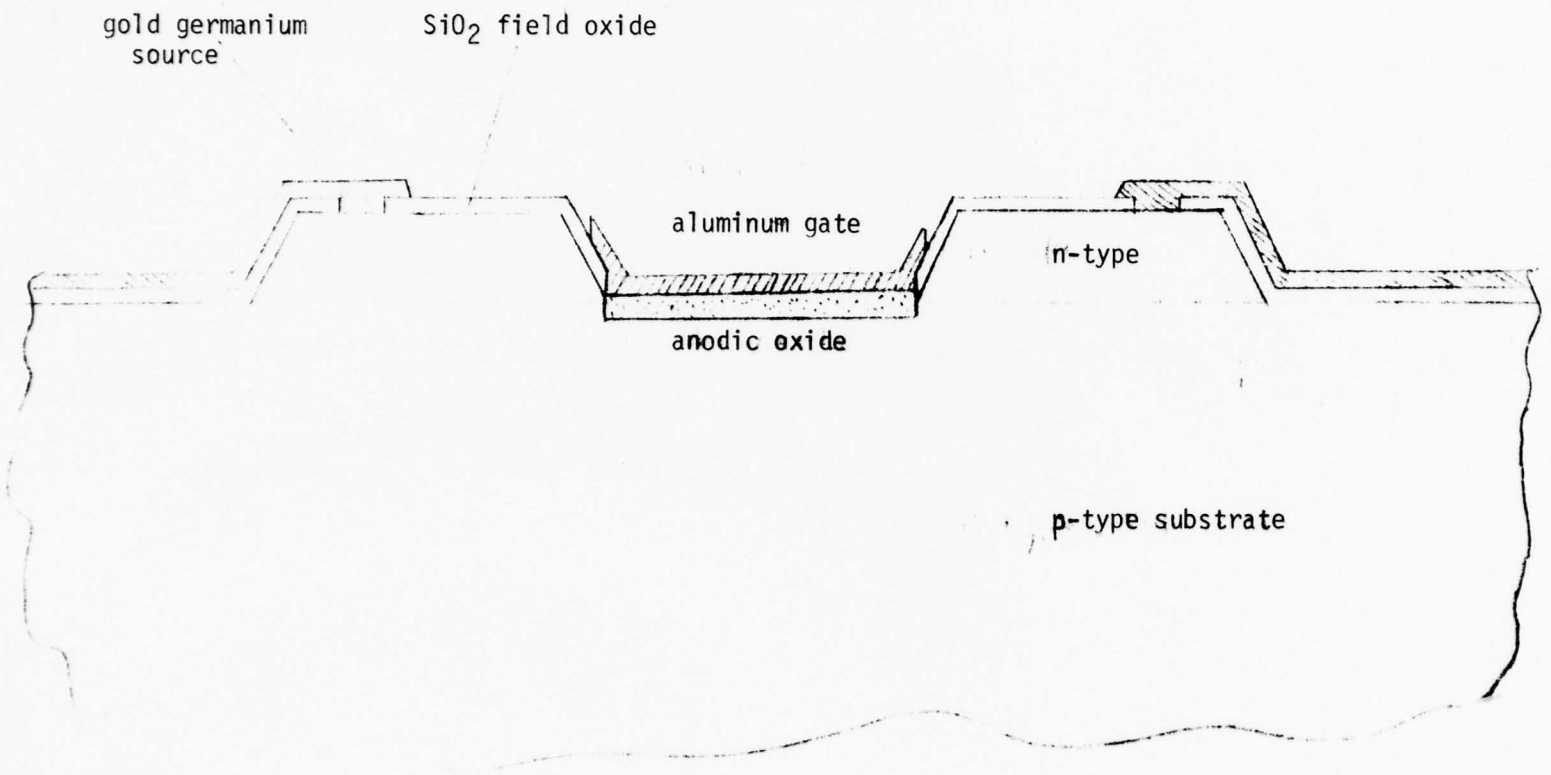


Figure 12 - Planar MISFET formed from epitaxial material.

is difficult. An etch which satisfies these criteria is HF:H_2O_2:H_2O, where the percentage concentration of HF is less than 6% and that of H_2O_2 is less than 10%. Above these values the etch begins to delineate defects in the material and loses its polishing quality. The etch rate is proportional to the H_2O_2 concentration and independent of the HF concentration as illustrated in Fig. 13. The etch rate is given by 483.3 K_p Å/min where K_p is the % concentration of H_2O_2.

In order to limit the attack of the HF on any SiO_2 layers, an etch having 1% HF concentration has been used with an H_2O_2 concentration of 3%, giving a convenient etch rate of 1450Å/min. Talystep profiles of a pair of etched mesas is shown in Fig. 14.

Since the etch rate is dependent only on the concentration of the HF, HCl and NaOH were substituted in turn in the etching mixture. 100 mls of 1% HCl added to 3 mls of H_2O_2 gave a similar behavior to the HF etch but with a slightly less polished surface. A 1% by weight solution of the NaOH with H_2O_2 gave a surprisingly different result as shown in the profile in Fig. 15. In this case, the mesas are much sharper and the etching solution is preferential. Because of this, the etch has applications in V-groove MISFET fabrication, Section 3.5.

3.3 Etching by Anodization

Anodization also offers a very convenient way of accomplishing the mesa etching since the thickness of grown anodic oxide on the p and n materials for the same applied potential is different and hence the color contrast can be used to show the exposure of the p-type layer.

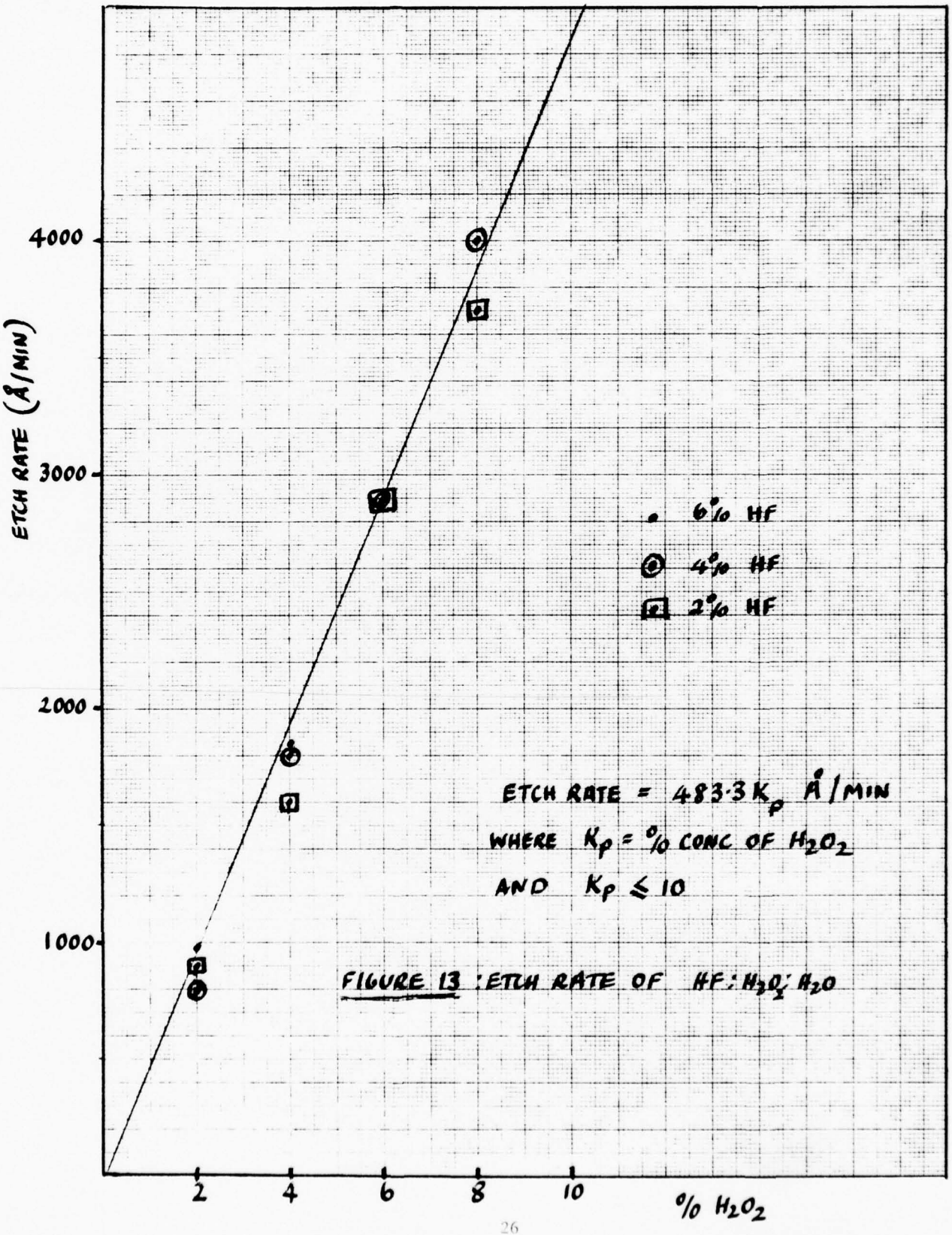


FIGURE 13 : ETCH RATE OF HF : H_2O_2 : H_2O

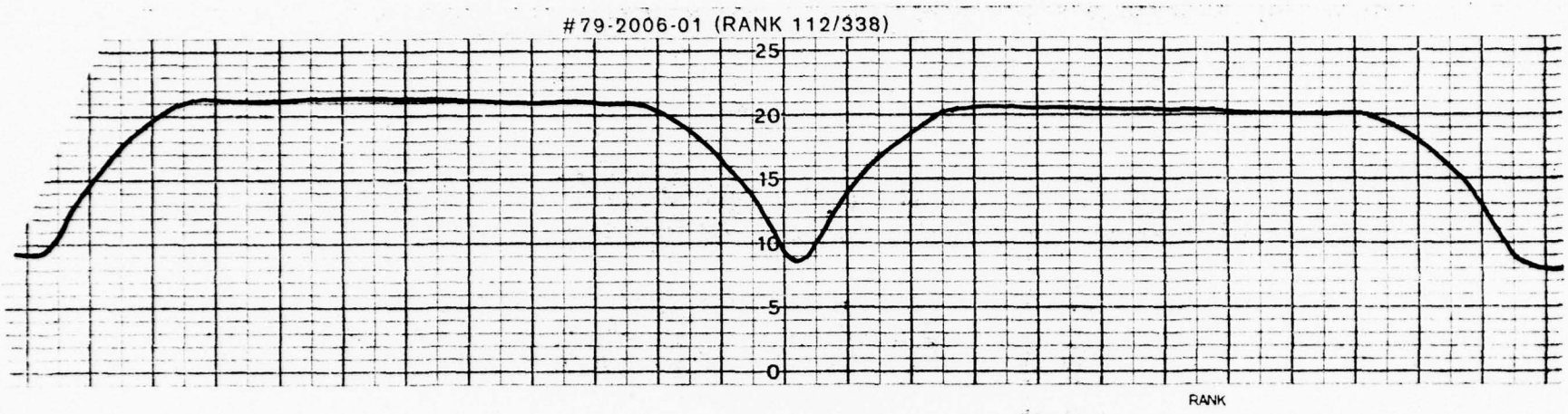


Figure 14 - Talystep profiles of mesas on CD3-R38-1β etched with $HF:H_2O_2:H_2O$ in the ratio 1:3:100. 1000Å/div vertical; 25000Å/div horizontal.

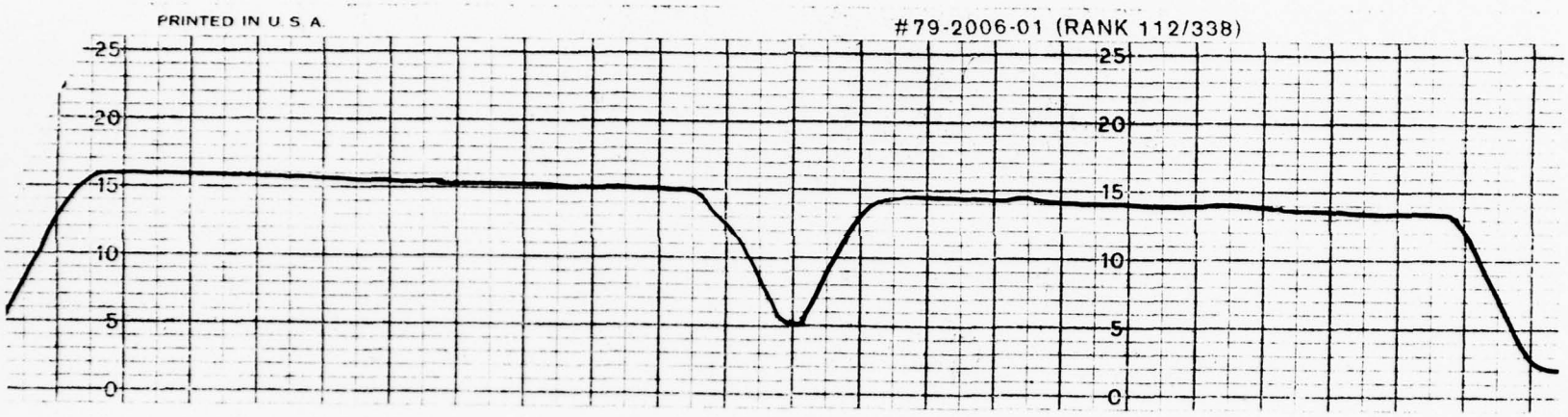


Figure 15 - Talystep profiles of mesas on CD3-R38-1B etched with $NaOH:H_2O_2:H_2O$ in the ratio 1:3:100. 1000Å/div vertical; 25000Å/div horizontal.

To illustrate this an n^+ substrate on which was grown sequentially an n^- layer 2.8 μm thick, a p-layer 3.5 μm thick and an n^+ layer 2.8 μm thick was used. The pattern for the source and drain areas was defined as shown in Fig. 16 and the remainder of the slice was anodized and the oxide removed in a number of steps until 1 μm of the surrounding material was removed. This leaves mesas 1 μm high but the total thickness of the n^+ region being 2.8 μm, the p-type layer was not yet exposed. The photoresist was then removed and the anodization-removal scheme continued in 70 volt steps (116Å of GaAs removed each time) until the pattern shown in Fig. 17 began to emerge.

Figure 17 shows two pieces taken from the same slice of epitaxially deposited material and which were etched and anodized separately. The center light area is a light blue color corresponding to an oxide thickness of 1190Å (52 volts). The region nearest the edge of the slice is a dark blue (940Å or 41 volts) and the transition region between these light and dark blue areas is still a darker blue corresponding to 800Å or 35 volts. The mesa pattern within the light blue area is also covered with 800Å of oxide.

The model for this variation in oxide thickness is outlined in Fig. 18. The epitaxial process leads to a variation in thickness of the final n^+ layer and the uniform removal of material eventually leads to three distinct regions. In Fig. 18a is depicted a mesa structure with the n^+ layer still intact around it. The anodizing solution is negatively biased with respect to the gallium arsenide and hence a depletion layer is formed at the surface of the sample and the voltage which can be sustained by this depletion layer is equal to

FIGURE 16 - SOURCE-DRAIN CONTACT PATTERN.

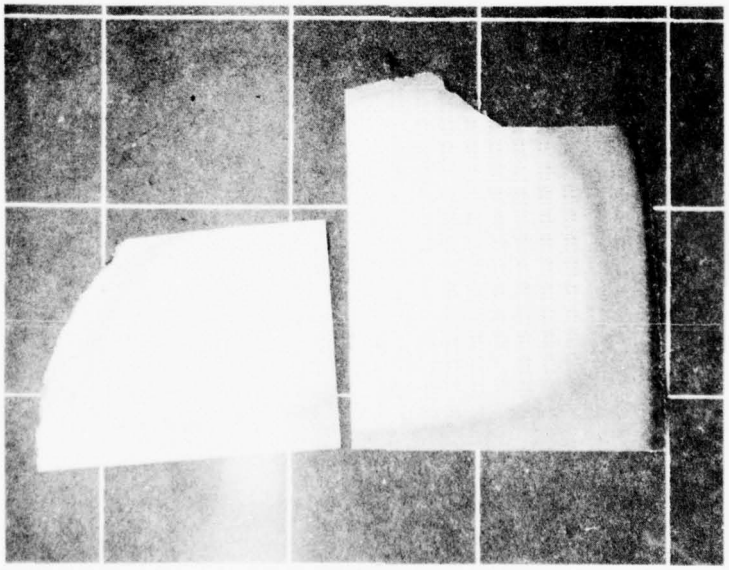


FIGURE 17 - ANODISED WAFERS SHOWING CONTRAST DUE TO P-LAYER EXPOSURE.

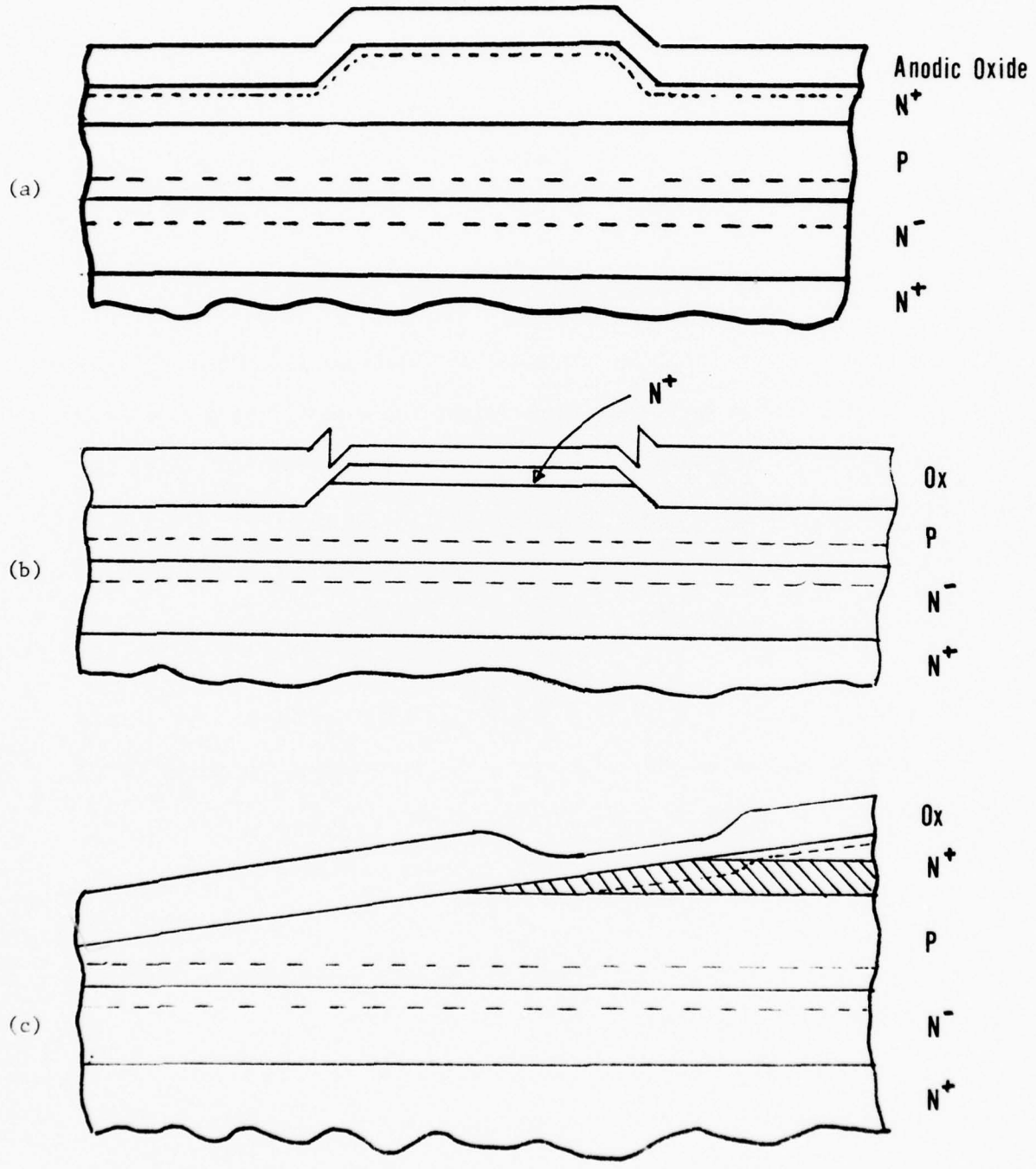


Figure 18 - Model for colors observed on anodized multi-epitaxial sample.

the breakdown voltage of the n layer (V_B). Between the n^+ and p layer is a forward biased junction with a negligibly small voltage drop. Between the p and n^- layers is a reverse biased junction with a large voltage drop V_{JR}. If the voltage applied between the back contact and the cathode (or solution) is V_A, then the voltage developed across the oxide (V_{OXN}) is

$$V_{OXN} = V_A - (V_B + V_{JR})$$

In Fig. 18b is shown a portion of the slice where the n^+ layer has been removed from the region surrounding the mesas. The p-type layer is exposed to the anodizing solution and there is no depletion layer at the surface in this case. Hence the voltage across the oxide in this case is

$$V_{OXP} = V_A - V_{JR}$$

which makes the oxide thicker by a value corresponding to V_B. From the differences in the oxide colors of the areas surrounding the mesas in the cases corresponding to Figs. 18a and 18b the value of V_B can be estimated at 17 volts, corresponding to a donor concentration of $9 \times 10^{16}/cm^3$ in the n-type layer. The oxide on the top of the mesa for Fig. 3b is thinner than that for Fig. 7a for the reason that is given in a discussion of Fig. 18c.

Figure 18c shows the exaggerated case of the transition between the conditions of Figs. 18a and 18b. As the n^+ gets thinner the depletion layer at the surface moves into a region of lower donor

concentration near the n-p interface and the width of the depletion layer increases with a corresponding increase (ΔV_B) in the breakdown voltage. The equation for the voltage (V_{OXI}) across the oxide is now

$$V_{OXI} = V_A - (V_B + \Delta V_B + V_{JR})$$

The color of the oxide gives a value of ΔV_B = 6 volts and $V_B + \Delta V_B$ = 23 volts corresponding to a donor concentration of $5 \times 10^{16}/cm^3$. The color at the top of the mesas is the same as that in the transition region giving the same value of donor concentrations for the source and drain contact regions.

The value of V_A was 65 volts leading to a value of V_{JR} of 13 volts which is a reasonable value for a junction occupying the total area of the slice.

MOS capacitance tests made on the areas of exposed p and residual n^+ have confirmed the above picture.

An important aspect of this work is that the above color variations only occur if the anodization is performed in the dark. Illuminating the sample produces a uniform color and oxide thickness. This is particularly important for the anodization of the gate areas for MISFET fabrication.

3.4 Fabrication Sequence

The first wafers of material were processed according to the schedule shown in Table II. The formation of the mesas and the thinning by anodization have already been discussed. Deposition of the gold - 12% germanium alloy (Step 5 in this fabrication sequence) was made over

TABLE II

INITIAL FABRICATION SEQUENCE FOR PLANAR DEVICE

1. Etch source-drain mesas ($NaOH:H_2O_2:H_2O$): Mask 648-1.
2. Thin layer to expose p-layer by anodization.
3. Deposit field oxide (0.5 μm SiO_2) by sputtering.
4. Open source-drain contact holes in field oxide: Mask 648-3.
5. Evaporate gold-germanium source drain contact metal and define by etching mask: 648-6 anneal contacts.
6. Etch gate region in field oxide: Mask 648-2.
7. Cover metal source and drain contacts with thick (1 μm) photoresist and open up regions for gate metal: Mask 648-5.
8. Anodize gate region to 50 volts (1050Å).
9. Evaporate gate metal 5000Å and strip resist, thereby defining gate metallization.
10. Anneal oxide.

the entire slice with the excess metal being removed by etching in Metex Aurostrip using a photoresist mask. A thin layer (200Å) of nickel was added to the layer in subsequent runs to avoid "balling-up" of the gold-germanium during alloying to the gallium arsenide. The nickel was pre-etched with dilute ferric chloride solution since it is attacked only slowly by Metex Aurostrip.

The anodization of the gate region was left as a late step in the fabrication sequence to avoid possible degradation during the processing required to apply the ohmic contacts. It was found, however, that the photoresist deposited in Step 7 of the fabrication sequence was not able to withstand the potential applied during the anodization (Step 8). Small pinholes in the resist allowed the anodizing solution to come into contact with the gold-germanium and, since the oxide is grown under constant current conditions, the current carried by these pinholes allowed only small (<10) voltages to be developed across the anodic oxide. Attempts were made to grow at constant (50) voltages but the large currents through the pinholes destroyed the resist. A series of devices made under these conditions had 20 volt (460Å) oxides which were very leaky.

In view of this problem, it was decided to form the gate oxide much earlier in the sequence at a time before the source and drain contacts are applied. The revised sequence is shown in Table III.

The sequence has the advantage that the gate oxide can be annealed and optimized early in the sequence without the problem of the gold-germanium contacts being completely alloyed into the gallium arsenide during the long annealing cycle (360°C for 3 hours[5]).

TABLE III

REVISED FABRICATION SEQUENCE FOR PLANAR DEVICE

1. Etch source-drain mesas ($NaOH:H_2O_2:H_2O$): Mask 648-1.
2. Thin layer to expose p-layer by anodization.
3. Deposit field oxide (0.5 μm SiO_2) by sputtering.
4. Open source-drain contact holes in field oxide: Mask 648-3.
5. Open up field oxide for gate region: Mask 648-2.
6. Cover slice with thick (1μm) photoresist and open up regions for gate metal: Mask 648-5.
7. Anodize gate region to 50 volts (1050Å).
8. Evaporate gate metal (5000Å) and strip resist, thereby defining gate metallization.
9. Anneal oxide.
10. Cover slice with thick (1μm) photoresist and open up regions for source-drain contacts.
11. Give light etch in NH_4OH to remove any oxide formed in openings during step 7.
12. Evaporate 5000Å AuGe and strip resist, thereby defining contact areas.

3.5 Results of Planar Device Fabrication

Five individual fabrication runs have been completed with the results shown tabulated in Table IV.

Wafer #D250676

The first wafer to be processed with mask set #648[6] was slice #D250676. This was a sulfur implant into p-type material through a 0.5 μm SiO_2 mask applied by RF sputtering. The energy of the singly charged sulfur ion was 140 KeV at a fluence of $10^{15}/cm^2$. The whole slice was then covered with a further 0.5 μm thick layer of sputtered SiO_2 and annealed at 790°C for 1 hour in nitrogen. A current-voltage plot of the back-to-back p-n junctions thus formed is shown in Fig. 19. The breakdown is soft, yielding 1 μA of current at 18 volts.

During this first fabrication sequence, the initial anodic oxide was stripped off in order to clean the gallium arsenide surface. A second anodic oxide was then grown and aluminum deposited through a photoresist mask to form the gate. The thickness of the photoresist and aluminum was 5000Å and 3000Å respectively. However, the resist was not thick enough to allow removal of the excess aluminum and hence the last two steps in the processing were repeated after etching off the aluminum and the gate oxide. Reoxidizing and redeposition of the gate resulted in the structure shown in Figs. 20 and 21. There is some misalignment of the gate but a more serious problem is the excessive depth to which the gate region has been etched, resulting in a discontinuity of the gate metal shown clearly in Fig. 21. This was confirmed by probing the sample.

TABLE IV

RESULTS OF PLANAR DEVICE FABRICATION

Identification #	Structure	Results
D250676	Sulfur implant into p substrate	Overetched channel region--no gate action.
CD3-R37-1A	Sulfur implant into 6 μm p with 8 μm n buffer layer.	Low source drain breakdown voltage.
CD3-R38-1A	Epitaxial 2.8 μm n^+, 3.5 μm p, 2.8 μm n^-, n^+ substrate.	Misaligned gate, overetched mesas, no gate action.
CD3-R38-1B	As above.	Working devices.
CD3-R39-1A	Epitaxial 1.9 μm n^+, 0.5 μm p, 3.8 μm n^-, n^+ substrate.	Misaligned gate, no gate action.

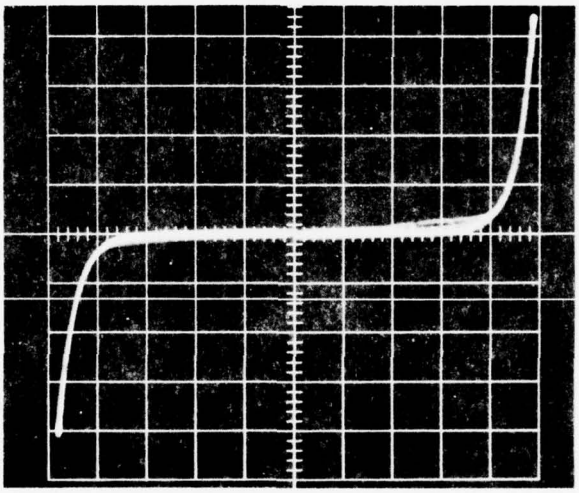


Figure 19 - I-V characteristic of back-to-back p-n junctions formed by sulfur implantation into wafer D250676.
5V/div horizontal; 10μA/div vertical.

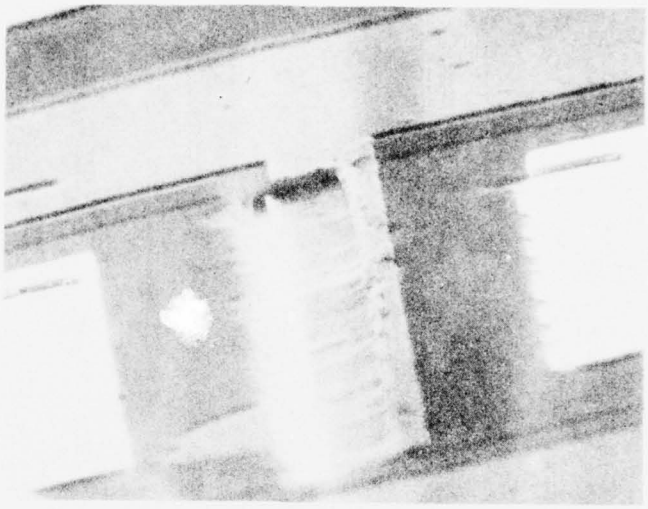


Figure 20

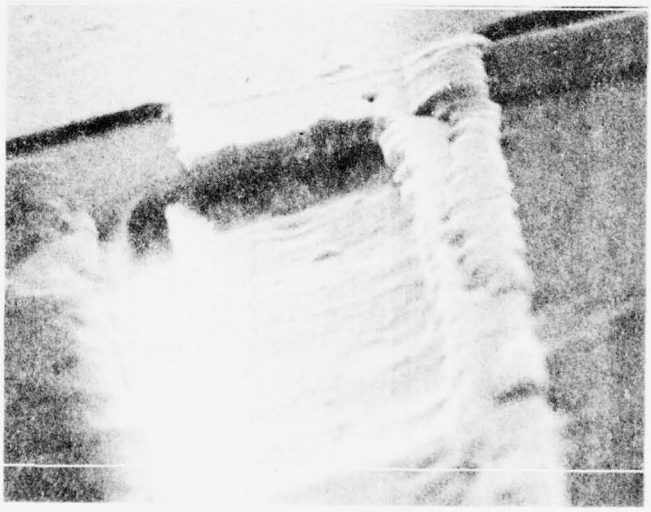


Figure 21

Scanning electron micrographs of completed devices on Slice D250676.

Wafer #CD3-R37-1A

This slice also had sulfur implanted n^+ source and drain areas, but in this case the implant was made into a p-type epitaxial layer on top of a thick (8 μm), highly doped n-type buffer layer. The source-drain current-voltage characteristic is shown in Fig. 22. The breakdown is very soft and occurs at only 1.6 volts. Devices were fabricated on this slice to develop the fabrication procedure, with no useful devices resulting.

Wafer #CD3-R38-1A

This wafer was a complex multilayer epitaxially grown (VPE) wafer, produced as part of the effort towards the vertical channel device. The p-layer was too thick for this purpose, however, and it was decided to use it for the planar device.

The mesas were etched using $HF:H_2O_2:H_2O$ in the ratio 4:4:92. During the etching process the photoresist lifted from the surface of the gallium arsenide, giving the mesas the shape indicated by the Talystep profile shown in Fig. 23 and the photomicrograph shown in Fig. 24. Because of the variation in the thickness of the n^+ layer across the slice, only a small region of the device was suitable for fabricating FET's. This is illustrated in Fig. 25. The problem is alleviated if the mesa edges are steeper. In addition, the alignments of the source and drain contacts with the slot in the field oxide and the gate metal with the anodic oxide are very poor (see Fig. 26) so that no gate action was observed.

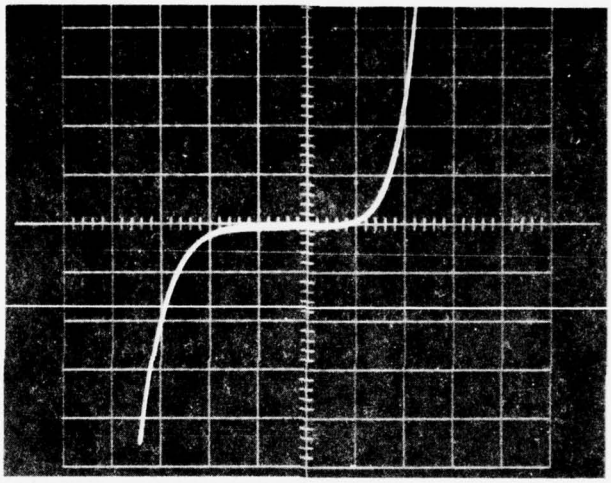


Figure 22 - I-V characteristics of back-to-back p-n junctions formed by sulfur implantation into Wafer CD3-R37-1A.
1V/div horizontal; 10μA/div vertical.

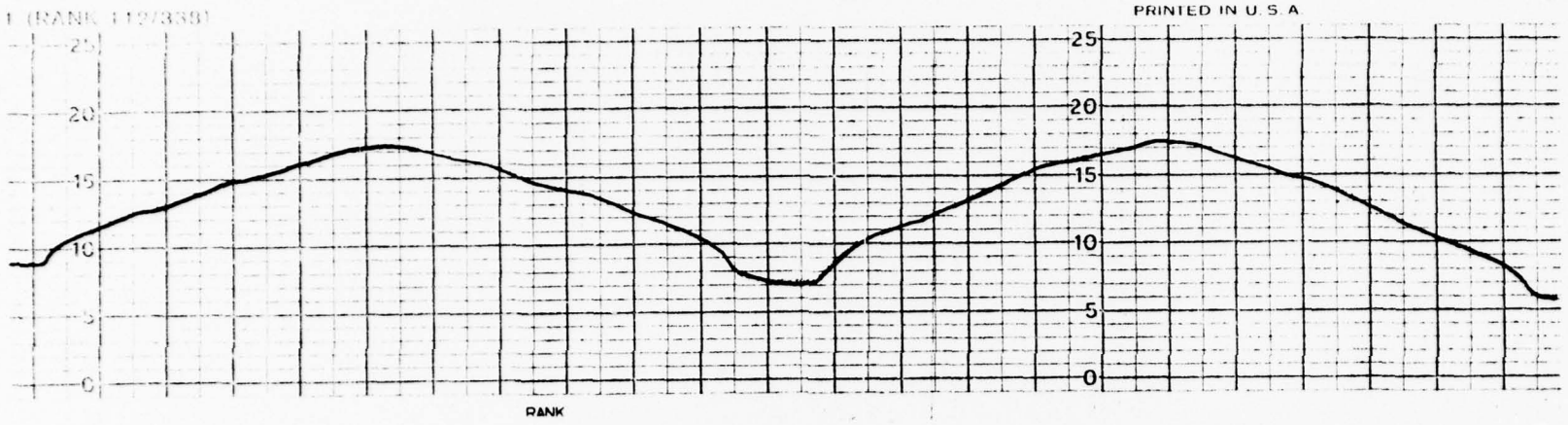


Figure 23 - Talystep profile of mesas on CD3-R38-1A etched with $HF:H_2O_2:H_2O$ in the ratio 4:4:92. 1000Å/div vertical, 25000Å/div horizontal.

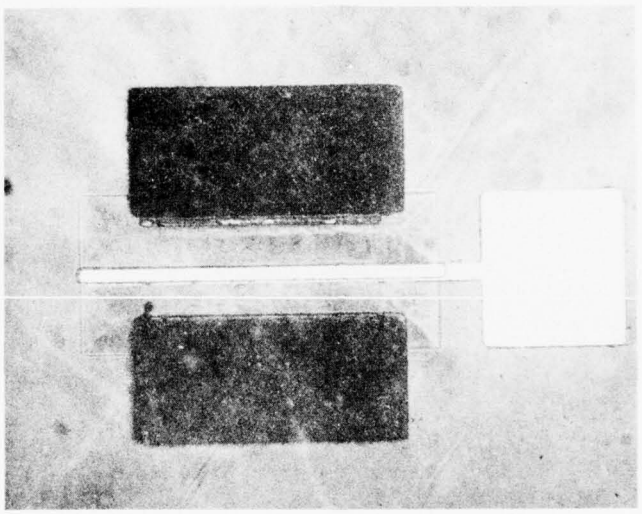
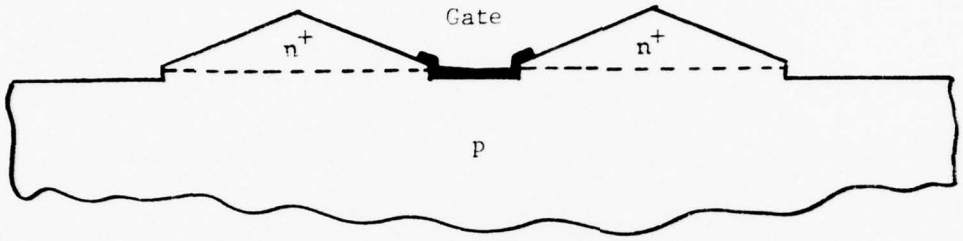
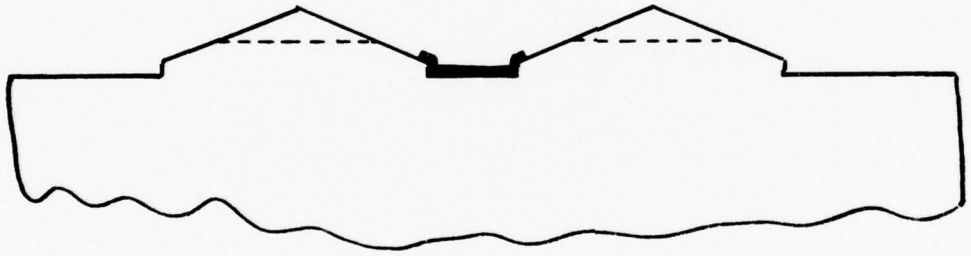


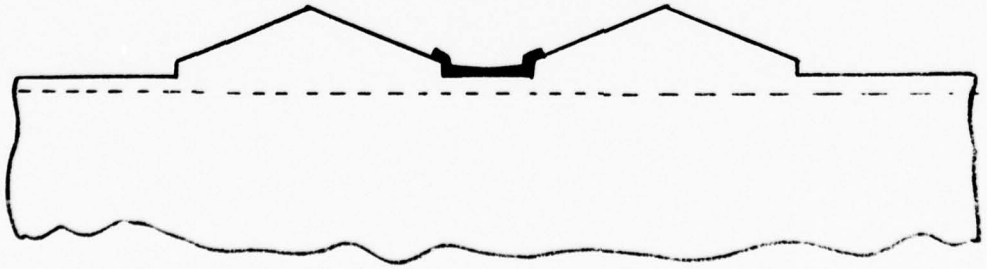
Figure 24 - Photomicrograph of device fabricated on Slice CD3-R38-1A showing pyramid-shaped mesas.



(a) Correct thickness for n^+ contacts.



(b) n^+ too thin.



(c) n^+ too thick.

Figure 25 - Problems due to pyramid-shaped mesas.

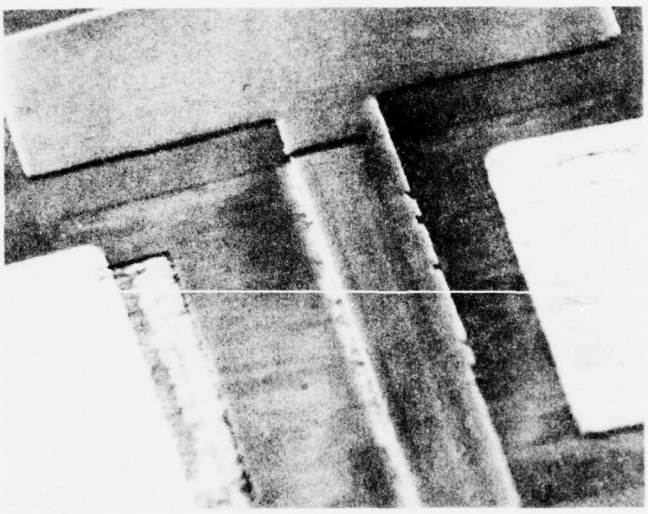


Figure 26 - Slice CD3-R38-1A showing misalignment of source and drain contacts and gate contact.

Wafer #CD3-R38-1B

This slice was the second half of the CD3-R38-1 slice and hence had the same epitaxial layer structure. The n^+ layer was etched using the $NaOH:H_2O_2:H_2O$ etch which was described earlier (Section 3.2). In addition, the surface of the gallium arsenide was treated with AP100[4] to reduce undercutting. A Talystep profile of the etched mesas was shown in Fig. 18 and scanning electron micrographs in Fig. 27. The edge of the mesas is now much sharper.

Devices were successfully fabricated on this slice and current-voltage characteristics are shown in Fig. 28. Figure 28a shows the characteristic in the dark while Fig. 28b shows the effect of strong illumination with a tungsten filament light source on the same device. The slice was annealed at 310°C in N_2 for 10 sec in order to form the ohmic contacts. Annealing of the anodic oxide has not been performed on this slice due to the fact that the aluminum gate contacts did not adhere well. The slice is presently being reprocessed through the anodization and gate deposition steps.

Wafer #CD3-R39-1A

This slice was processed in parallel with the previous slice but there was no gate action due to misalignment over the anodic oxide. This can be seen in Fig. 29. This slice is also being reprocessed.

3.6 V-Groove VMIST

Work was also carried out on the fabrication of a V-groove transistor as a first step towards the realization of a vertical channel

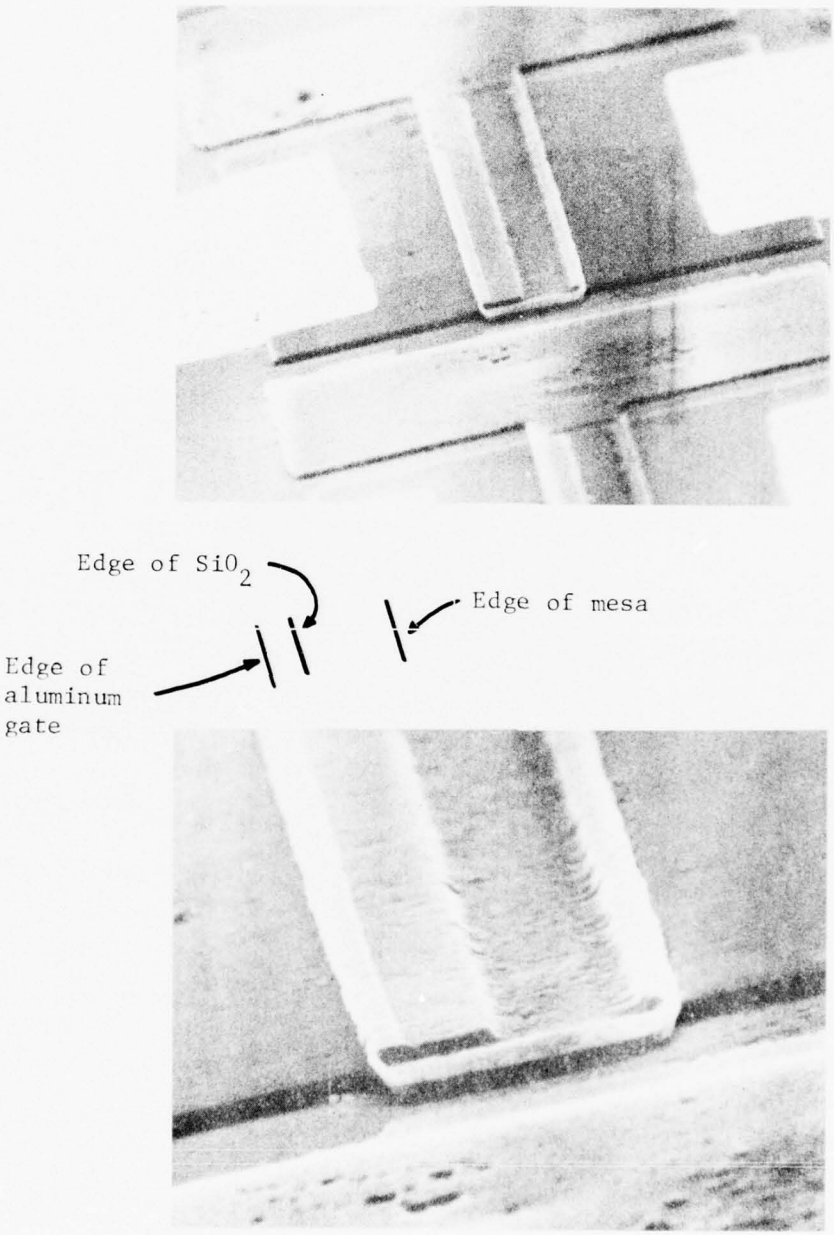


Figure 27 - Scanning electron micrograph of Slice CD3-R38-1B.

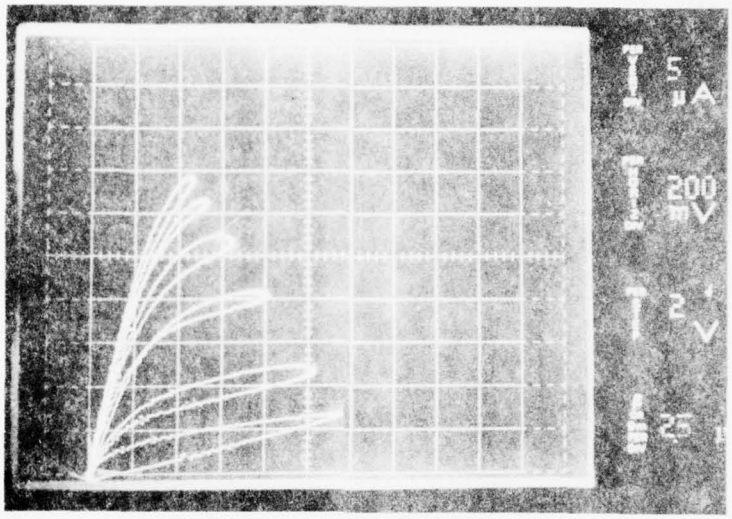
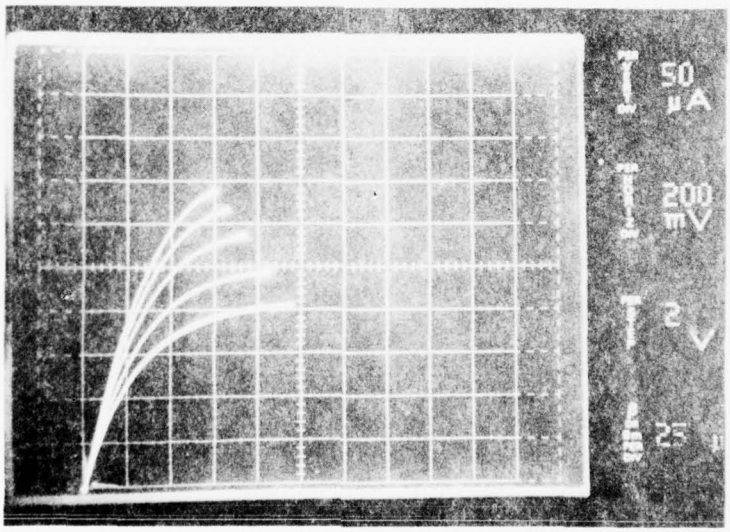


Figure 28a



I-V Characteristics of Transistors formed on Slice CD3-R38-1B.

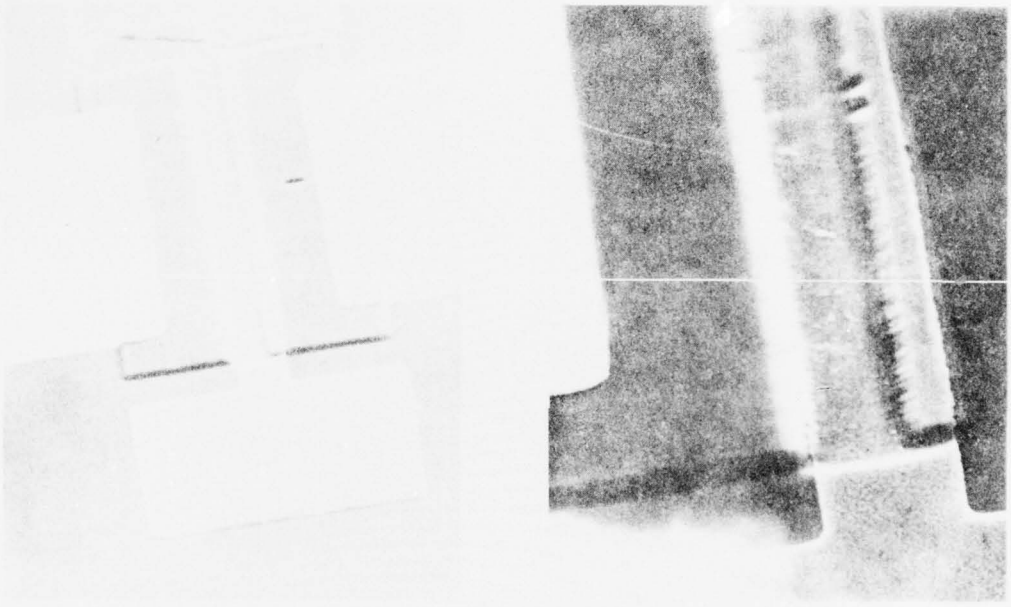


Figure 29 - Scanning electron micrograph of Slice CD3-R39-1A, showing misalignment of gate contact over anodic oxide.

VMIST device[7]. A cross section of the device is shown in Fig. 30. Bromine methanol was used to etch the V-groove and a scanning electron micrograph of the groove is shown in Fig. 31. The angle of the etched plane forming the sides of the V-groove with the <100> surface is 45° which corresponds to the angle between the <100> and <110> planes. Thus the etched planes are <110>.

The main problem with the bromine-methanol etch is that it accentuates defects in the material. The $NaOH:H_2O_2:H_2O$ (1:3:100) etch described in Section 3.2 was used to etch a V-groove using a 0.5 μm thick SiO_2 masking layer on top of a n-p-semi-insulating GaAs wafer. The scanning electron micrographs of the resulting structures are shown in Fig. 32. In Figs. 32a and b, the oxide has been left in place and the interesting corrigated structure is a result of stress relief. The gap between SiO_2 overhangs is 2.8 μm. In Figs. 32c and d, the oxide has been removed. In the wider oxide openings shown in Fig. 32d and Fig. 33, the etch has penetrated to the interface between the epitaxial layer and the substrate. In micrographs 32c and d, the p-type epitaxial layer is visible as a light band at the top of the vee. The thickness of the p-layer is 2.5 μm.

The angle between the planes of the V-groove is 105° which indicates that the pattern is not perfectly aligned along the <110> direction. Etching along openings in the SiO_2, which are perpendicular to the ones which yield the V-groove, gives the undercut structure shown in Fig. 34. Further experiments are planned to exploit the properties of this etch.

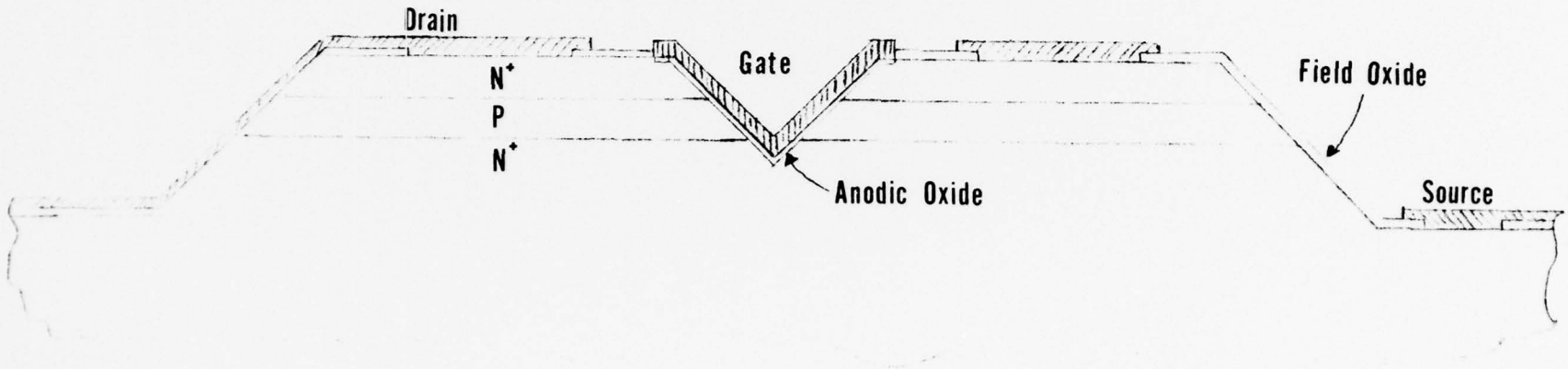


Figure 30 - Proposed V-groove device.

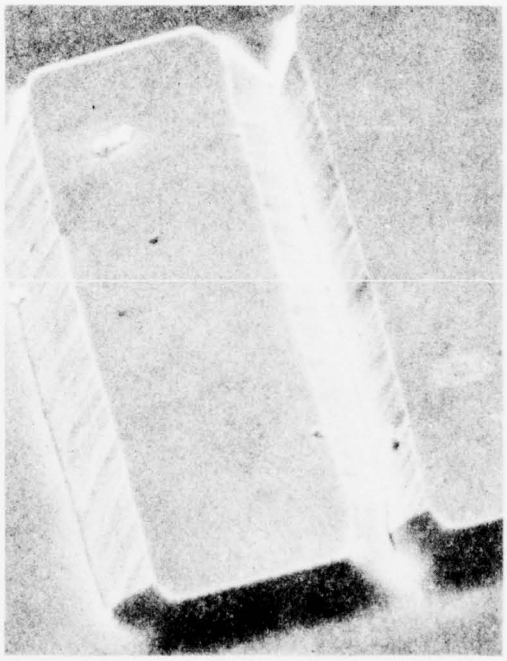
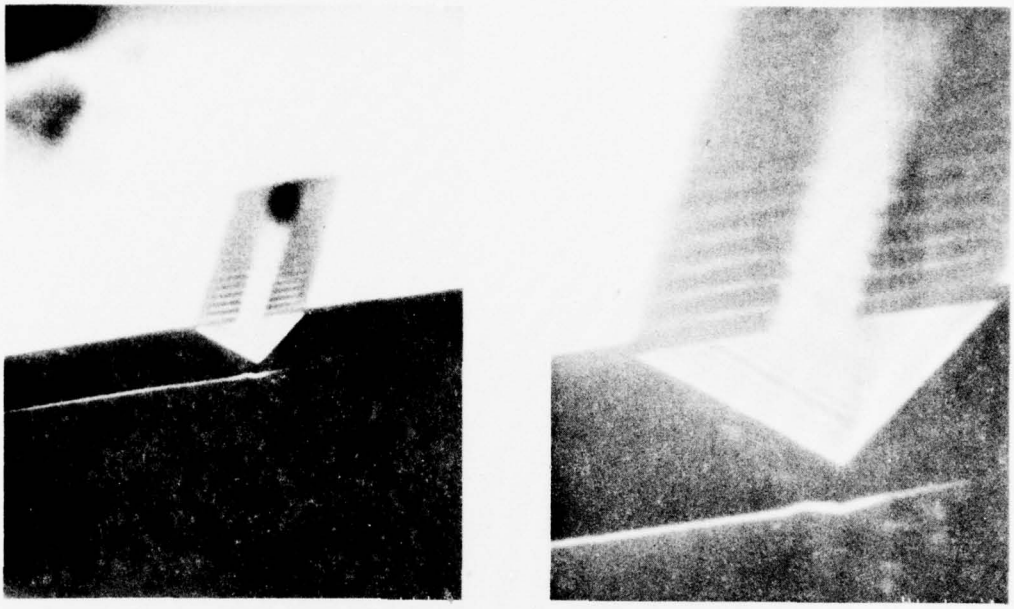


Figure 31 - V-groove obtained with bromine-methanol etch.



(a) (b)

(c) (d)

Figure 32 - V-grooves obtained with $NaOH:H_2O_2:H_2O$ etch.

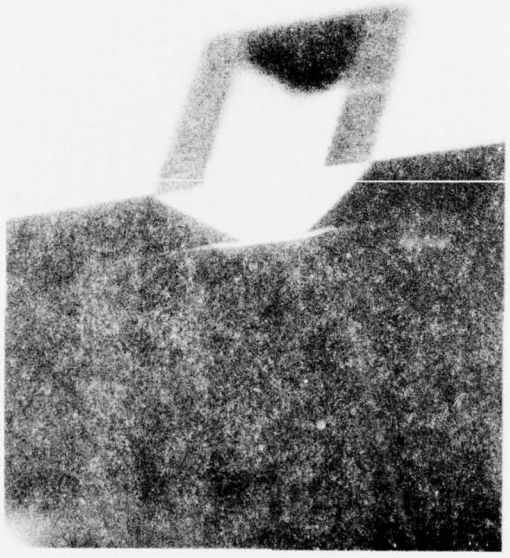
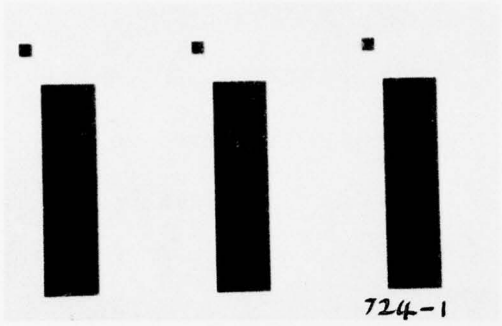


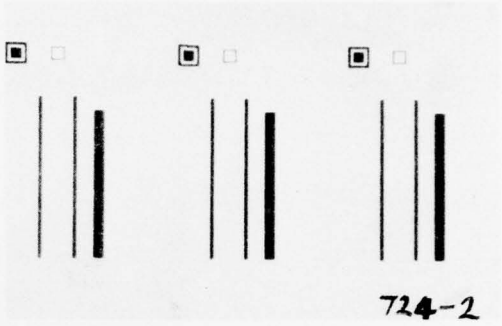
Figure 33 - Wide V-groove obtained with $NaOH:H_2O_2:H_2O$ etch.

Figure 34 - Etch pattern obtained at 90° to V-groove direction in <100> surface.

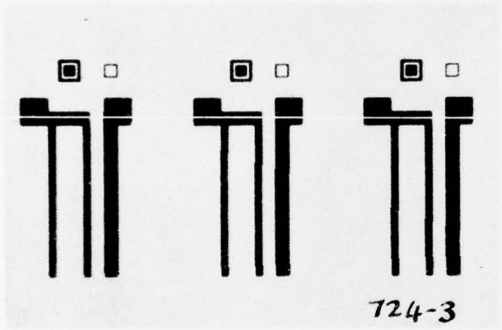
A mask set has been designed and fabricated and is shown in Fig. 35. Mask #724-5 has five groove widths from which can be selected the one appropriate to the epitaxial layer thicknesses. They are placed on the same mask so that if subsequent alignments of a longer or shorter gate is required during fabrication, the gate length can be selected from the same field on the mask, thereby eliminating any step and repeat errors.



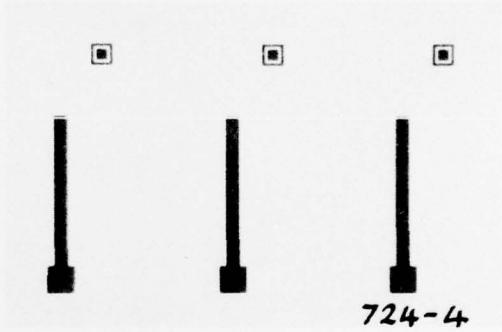
MESA



SOURCE-DRAIN CONTACT OPENINGS



SOURCE-DRAIN CONTACT METAL



GATE METAL

V-GROOVE OPENINGS

Figure 35 - Mask set for V-groove devices.

4. CONCLUSION

A great deal of technological progress has been made during this phase of the program. The various processes have been combined to fabricate a planar MISFET device as the first step towards a vertical channel VMIST device.

The best results came from wafers where the necessary doping had been produced by epitaxial growth. Ion implantation to produce n^+ contacts is being studied further. The most important application is in producing deep p-type implants to ground the substrate of the vertical channel device. The available energy (300 KeV) for the zinc implants appears to be insufficient to penetrate the necessary distance. Beryllium is now being studied as a possible alternative. Although devices have been successfully fabricated, the properties of the gate oxide have not yet been optimized by annealing at the completed device stage. More effort will be needed in this area.

Etchants have been developed for the V-groove devices which represent the next step towards the VMIST device. Further studies on relieving the internal stresses of the SiO_2 overhangs are also needed.

5. FUTURE WORK

Work is continuing on the planar MISFET device to bring it to its logical conclusion, together with fabrication of the V-groove device in order to take advantage of the narrow gate lengths that can be achieved with this configuration. We propose also to continue investigating the problems involved in the additional technology required to fabricate the vertical channel MISFET device which was shown in Fig. 1. Of necessity, this will require additional development of multi-epitaxial layer structures of uniform and controlled thickness and concentration levels in GaAs.

The following problems will receive special attention:

1. Optimization of anodic oxide in device structures.
2. Development of epitaxial growth for vertical device structures.
3. Development of V-groove structures with special attention to orientation effects.
4. Investigation of vertical channel MISFET geometrics.
5. Development of deep p-type implantations for MISFET substrate grounding.
6. Analysis and optimization of device structures.

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